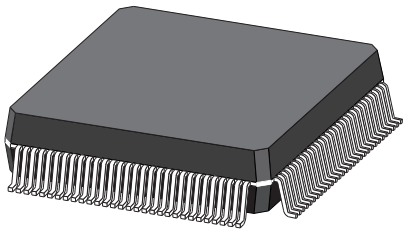
Digital Semiconductor

DECchip 21041 PCI Ethernet LAN Controller

Product Brief

March 1995



Description

The DECchip 21041 PCI Ethernet LAN Controller is a single-chip master, direct memory access (DMA) Ethernet LAN controller with a direct interface to the PCI local bus. It supports full-duplex operation, and its unique design is optimized to reduce the host bus utilization.

The DECchip 21041 is highly integrated to support 10BASE5, 10BASE-T, or 10BASE2 network connections. It is a high-performance device designed for PCI-based systems. The DECchip 21041 provides a direct interface to a 64KB, 128KB or 256KB boot ROM. It supports both PCI 3.3-volt and 5.0-volt signaling environments and a power-down mode for energy conservation. The DECchip 21041 is supported by a variety of software drivers and therefore offers a complete solution for all the leading networking environments.

Features

- Offers a single-chip Ethernet controller for PCI local bus:
  - Provides glueless connection to PCI bus
  - Contains an onchip integrated attachment unit interface (AUI) port and a 10BASE-T transceiver
- Implements the same architecture as the DECchip 21040 to allow use of unified drivers*
- Supports full-duplex operation and IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex network environments*
- Provides upgradable boot ROM (flash or EEPROM) interface of 64KB, 128KB, or 256KB*
- Contains MicroWire EEPROM interface for Ethernet ID address and, optionally, other system parameters*
- Provides PCI clock speed up to 33 MHz, with no wait states on PCI master operation
- Enables powerful onchip DMA with programmable burst sizes up to 32 longwords, providing for low CPU utilization
- Implements unique, patent-pending intelligent arbitration between DMA channels preventing underflow or overflow and optimized for full-duplex operation
- Incorporates a 16-bit, general-purpose timer*
- Contains two large (256-byte) independent receive and transmit FIFOs
- Supports either big- or little-endian byte ordering
- Implements JTAG compatible test-access port with boundary-scan pins
- Provides full support of IEEE 802.3, ANSI 8802-3, and Ethernet standards
- Offers a unique, patented solution to Ethernet capture-effect problem
- Contains a variety of flexible address filtering modes
- Supports seven LEDs: Receive, Receive Address Match, Transmit, Transmit Jabber, Collision, LinkPass, and Polarity*
- Enables automatic detection and correction of 10BASE-T receive polarity
- Enables full autosensing between 10BASE-T, 10BASE2, and 10BASE5 ports*
- Provides external and internal loopback capability
- Low power 3.3-V CMOS process technology
- Interfaces to 5.0-V or 3.3-V logic
- Provides a software-controllable power-saving mode*
- Supports PCI 5.0-V and 3.3-V signaling environments*

*Asterisk indicates DECchip 21041 feature enhancements that are not available in the DECchip 21040.

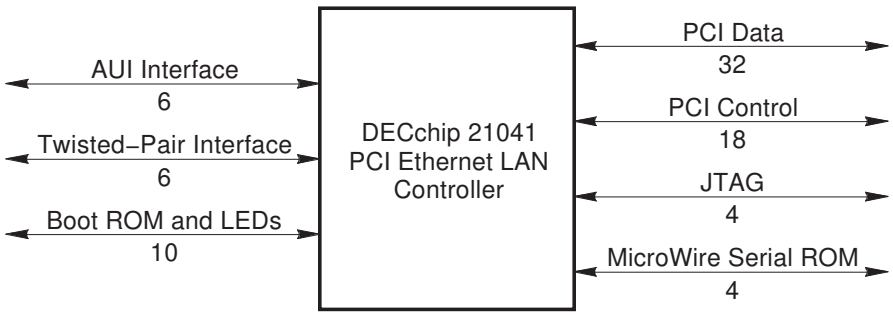
DECchip 21041 Microarchitecture

The DECchip 21041 communicates with the host processor using onchip command and status registers, and a shared host memory area. Most of the required setup and initialization is done after power-up. The DECchip 21041 software interface and data structures are optimized to remove load from the host CPU and to allow for maximum flexibility in the buffers' descriptor management. In normal operation, very little host CPU intervention is required. The DECchip 21041 filters out runt frames and does not need to reload the FIFO following collision, thereby minimizing bus traffic.

On the network side, the DECchip 21041 provides a direct interface to the AUI and 10BASE-T connections. The DECchip 21041 sustains full-line speed reception and transmission. The dual onchip 256-byte FIFOs and the internal microarchitecture provide complete support for full-duplex operation.

Figure 1 shows the functional groups of the DECchip 21041 interface pins.

Figure 1 DECchip 21041 Pin Interface



System Applications

The DECchip 21041 is optimized for PCI-based systems. A direct connection to 10BASE-T is made through the twisted-pair port. From the AUI port, the DECchip 21041 can connect to 10BASE2, 10BASE5, or 10BASE-F using the appropriate media access unit (MAU) and circuitry. The DECchip 21041 is a high-performance, highly integrated solution for a variety of applications, such as:

- Minimum-size, cost-effective PCI-to-Ethernet adapter card
- Minimum space, cost-effective integrated PCI motherboard controller
- PCI-based, switched Ethernet or multiport Ethernet bridge

Figure 2 shows the PCI-to-Ethernet adapter card using the DECchip 21041.

Figure 3 shows the PCI motherboard system with the DECchip 21041.

Figure 4 shows the PCI-based bridge and switch using the DECchip 21041.

Figure 2 PCI-to-Ethernet Adapter Card

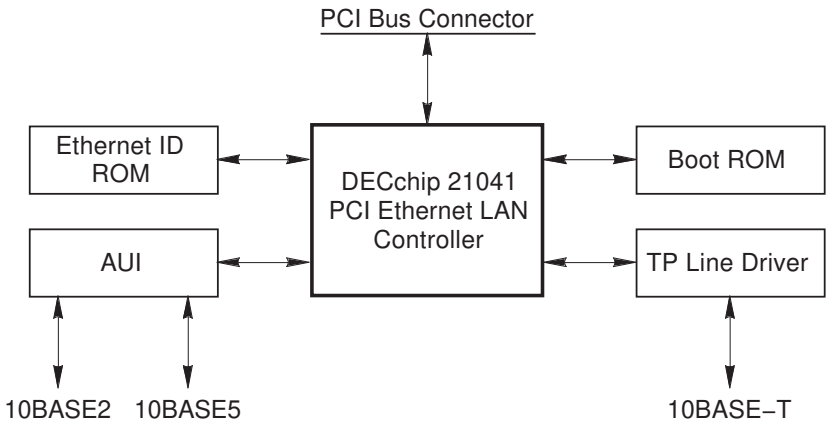


Figure 3 PCI Motherboard System

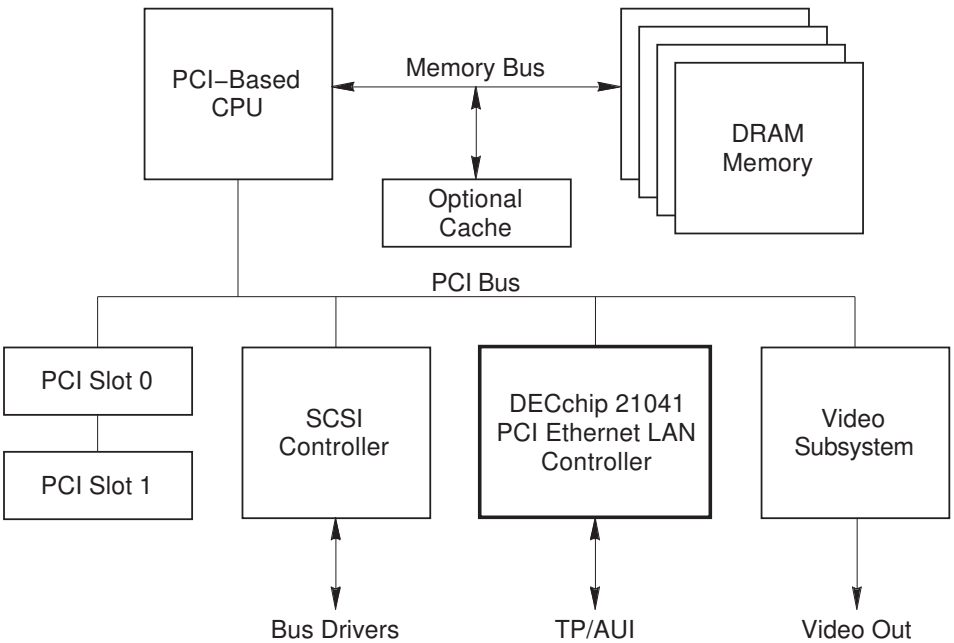
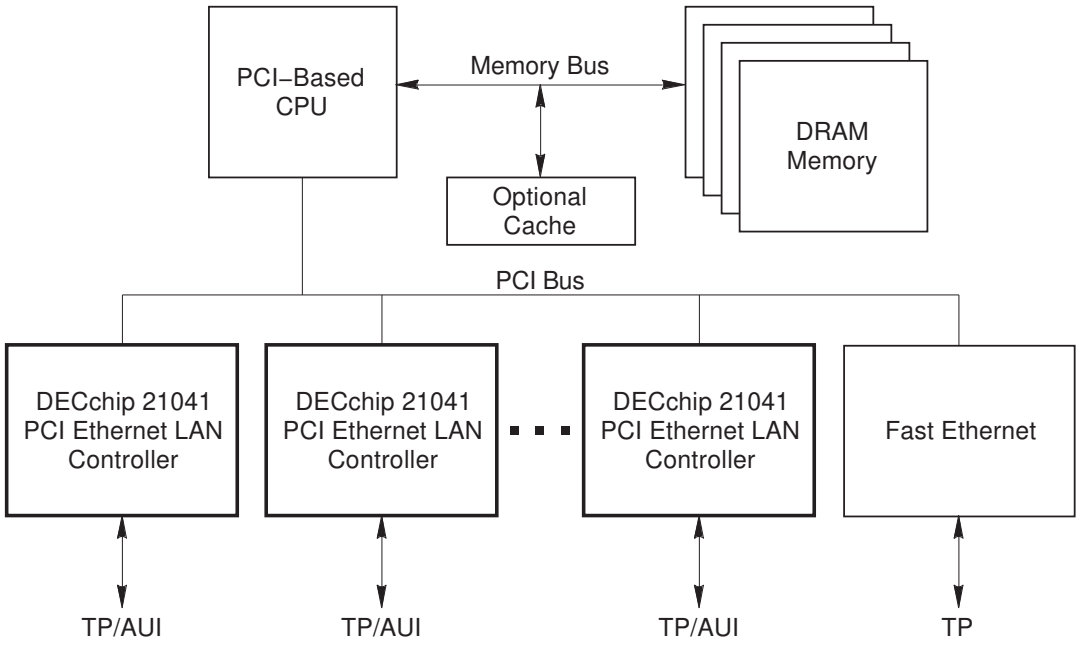


Figure 4 PCI-Based Bridge and Switch



Complete Solution

The DECchip 21041 evaluation board kit provides all the tools necessary for hardware engineers to design a standard PCI Ethernet controller board for a variety of products.

The kit includes a PCI evaluation board with 10BASE-T, 10BASE5, and 10BASE2 connections. It also includes complete driver and documentation sets, as well as schematics and gerber files.

Software drivers used for network operation will be provided for NetWare, PATHWORKS, SCO UNIX, and Microsoft's LAN Manager, Windows NT, Windows 95, and Windows for Workgroups.

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Characteristics	
Characteristic	**Specification**
Power supply	Vdd = 3.3 V Vdd_clamp = 5 V or 3.3 V
Operating temperature	0°C to 70°C
Storage temperature range	–55°C min, +125°C max
Power dissipation @ Vdd = 3.3 V and PCI clock frequency = 33 MHz	0.5 W
Package	120-pin PQFP

For More Information

To learn more about the availability of the DECchip 21041 and evaluation board kit, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

1-800-332-2717
1-800-332-2515 (TTY)

Outside North America, call:

+1-508-568-6868

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