DOCUMENT NUMBER:
EC-QHV2A-TE

DECchip 21130 EVALUATION BOARD KIT (EB130)

This Document Contains Schematics (CS), a Mechanical Drawing (MD), and Unit Assembly Drawings (UA) for the EB130 ** PRELIMINARY RELEASE **.

CONTENTS:

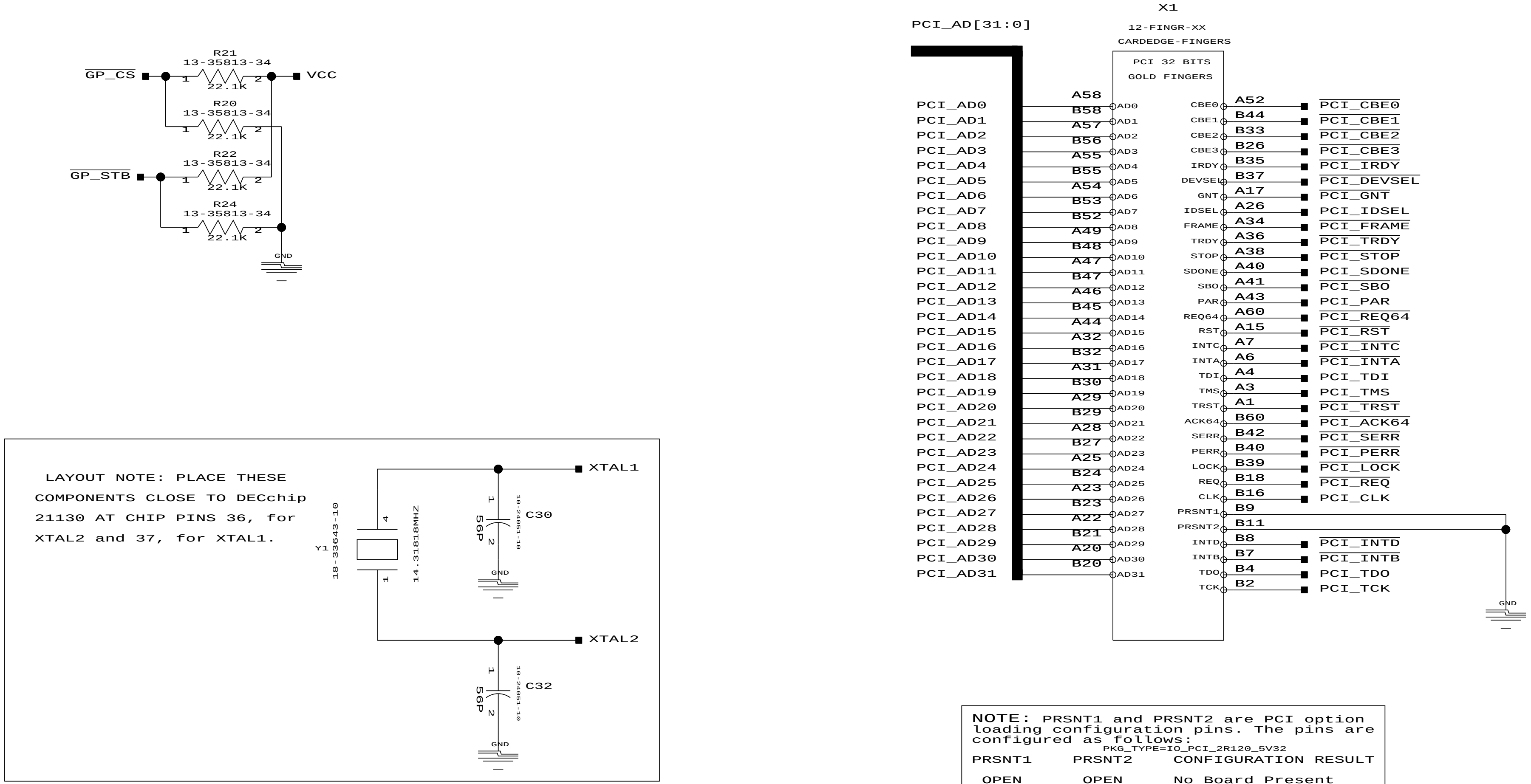
REVISION		
CHK	CHANGE NO.	REV

digital

DRN. P. CAMPOS	DATE	ENG. M. SULLIVAN	DATE
CHK'D.	DATE	BOARD LOCATION:	
USRA:		SHEET 1 OF 8	
FIRST USED ON OPTION/MODEL:		TOP DOCUMENT NUMBER: K-DD-5424315-0-0	

TITLE: 21130 EVAL BOARD			
SIZE	CODE	NUMBER	REV.
B	CS	5424315-0-1	AX01

PCI BUS I/O GOLD FINGERS



NOTE: PRSNT1 and PRSNT2 are PCI option loading configuration pins. The pins are configured as follows:

PKG_TYPE=IO_PCI_2R120_5V32

PRSNT1	PRSNT2	CONFIGURATION RESULT
OPEN	OPEN	No Board Present
GND	OPEN	25 Watt Max Board
OPEN	GND	15 Watt Max Board
GND	GND	7.5 Watt Max Board

REVISION		
CHK	CHANGE NO.	REV

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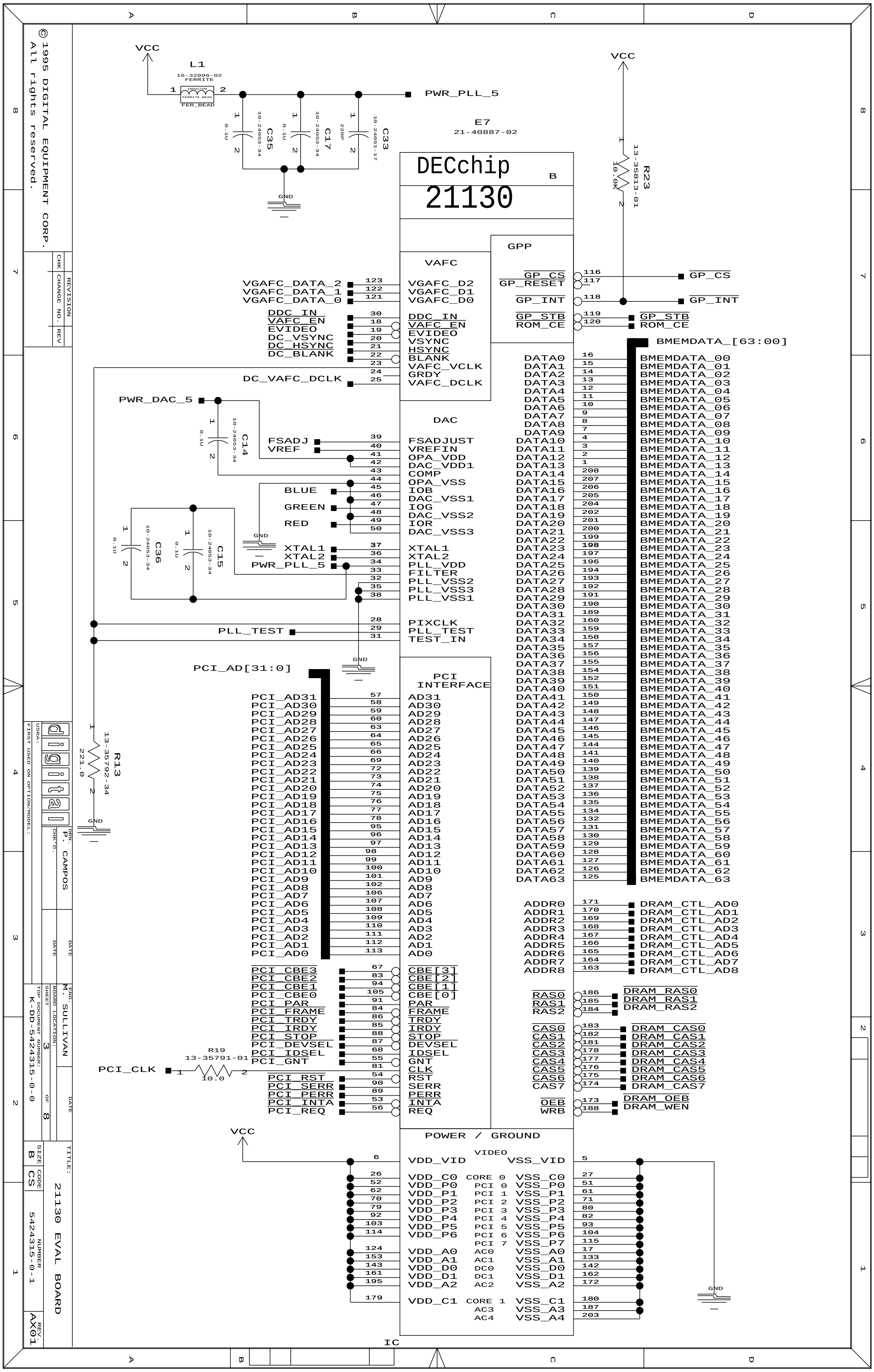
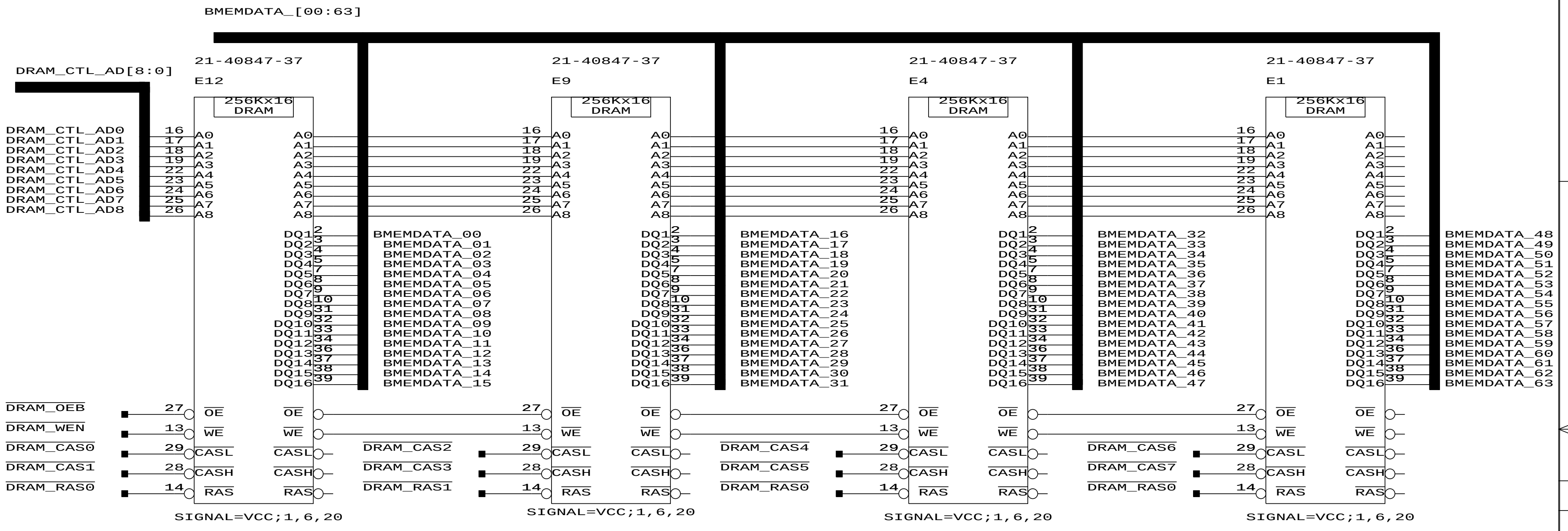
DRN. P. CAMPOS DATE
CHK'D. DATE
ENG. M. SULLIVAN DATE
BOARD LOCATION:
SHEET 2 OF 8
USRA:
FIRST USED ON OPTION/MODEL:
TOP DOCUMENT NUMBER: K-DD-5424315-0-0

TITLE: 21130 EVAL BOARD

SIZE B | CODE CS | NUMBER 5424315-0-1 | REV. AX01


VCC
L1
16-32996-02
FERRITE
FER_BEAD
PWR_PLL_5
C35 10-24053-34 0.1U
C17 10-24053-34 0.1U
C33 10-24051-17 220P
GND
E7
21-40887-02
DECchip 21130
B
R23
13-35813-01
10.0K
GPP
GP_CS
GP_RESET
GP_INT
GP_STB
ROM_CE
VAFC
VGAFC_DATA_2
VGAFC_DATA_1
VGAFC_DATA_0
VGAFC_D2
VGAFC_D1
VGAFC_D0
DDC_IN
VAFC_EN
EVIDEO
DC_VSYNC
DC_HSYNC
DC_BLANK
VSYNC
HSYNC
BLANK
VAFC_VCLK
GRDY
DC_VAFC_DCLK
VAFC_DCLK
PWR_DAC_5
C14 10-24053-34 0.1U
DAC
FSADJ
VREF
FSADJUST
VREFIN
OPA_VDD
DAC_VDD1
COMP
OPA_VSS
BLUE
GREEN
RED
IOB
DAC_VSS1
IOG
DAC_VSS2
IOR
DAC_VSS3
C36 10-24053-34 0.1U
C15 10-24053-34 0.1U
XTAL1
XTAL2
PLL_VDD
FILTER
PLL_VSS2
PLL_VSS3
PLL_VSS1
PIXCLK
PLL_TEST
TEST_IN
BMEMDATA_[63:00]
DATA0 … DATA63
BMEMDATA_00 … BMEMDATA_63
PCI_AD[31:0]
PCI INTERFACE
PCI_AD31 … PCI_AD0
AD31 … AD0
R13
13-35792-34
221.0
PCI_CBE3
PCI_CBE2
PCI_CBE1
PCI_CBE0
CBE[3]
CBE[2]
CBE[1]
CBE[0]
PCI_PAR
PCI_FRAME
PCI_TRDY
PCI_IRDY
PCI_STOP
PCI_DEVSEL
PCI_IDSEL
PCI_GNT
PAR
FRAME
TRDY
IRDY
STOP
DEVSEL
IDSEL
GNT
CLK
R19
13-35791-01
10.0
PCI_CLK
PCI_RST
PCI_SERR
PCI_PERR
PCI_INTA
PCI_REQ
RST
SERR
PERR
INTA
REQ
ADDR0 … ADDR8
DRAM_CTL_AD0 … DRAM_CTL_AD8
RAS0
RAS1
RAS2
DRAM_RAS0
DRAM_RAS1
DRAM_RAS2
CAS0 … CAS7
DRAM_CAS0 … DRAM_CAS7
OEB
WRB
DRAM_OEB
DRAM_WEN
POWER / GROUND
VIDEO
VDD_VID
VSS_VID
VDD_C0
CORE 0
VSS_C0
VDD_P0 … VDD_P6
PCI 0 … PCI 7
VSS_P0 … VSS_P7
VDD_A0
VDD_A1
VDD_D0
VDD_D1
VDD_A2
AC0
AC1
DC0
DC1
AC2
VSS_A0
VSS_A1
VSS_D0
VSS_D1
VSS_A2
VDD_C1
CORE 1
AC3
AC4
VSS_C1
VSS_A3
VSS_A4
IC
REVISION
CHK
CHANGE NO.
REV
digital
USRA:
FIRST USED ON OPTION/MODEL:
DRN: P. CAMPOS
CHK'D:
DATE
ENG: M. SULLIVAN
BOARD LOCATION:
SHEET 3 OF 8
TOP DOCUMENT NUMBER:
K-DD-5424315-0-0
TITLE: 21130 EVAL BOARD
SIZE B
CODE CS
NUMBER 5424315-0-1
REV. AX01

DRAM BANK 0



NOTE: 1MB DRAM SOLDERED TO BOARD,
OPTIONAL DRAM SELECTION SOCKETED.

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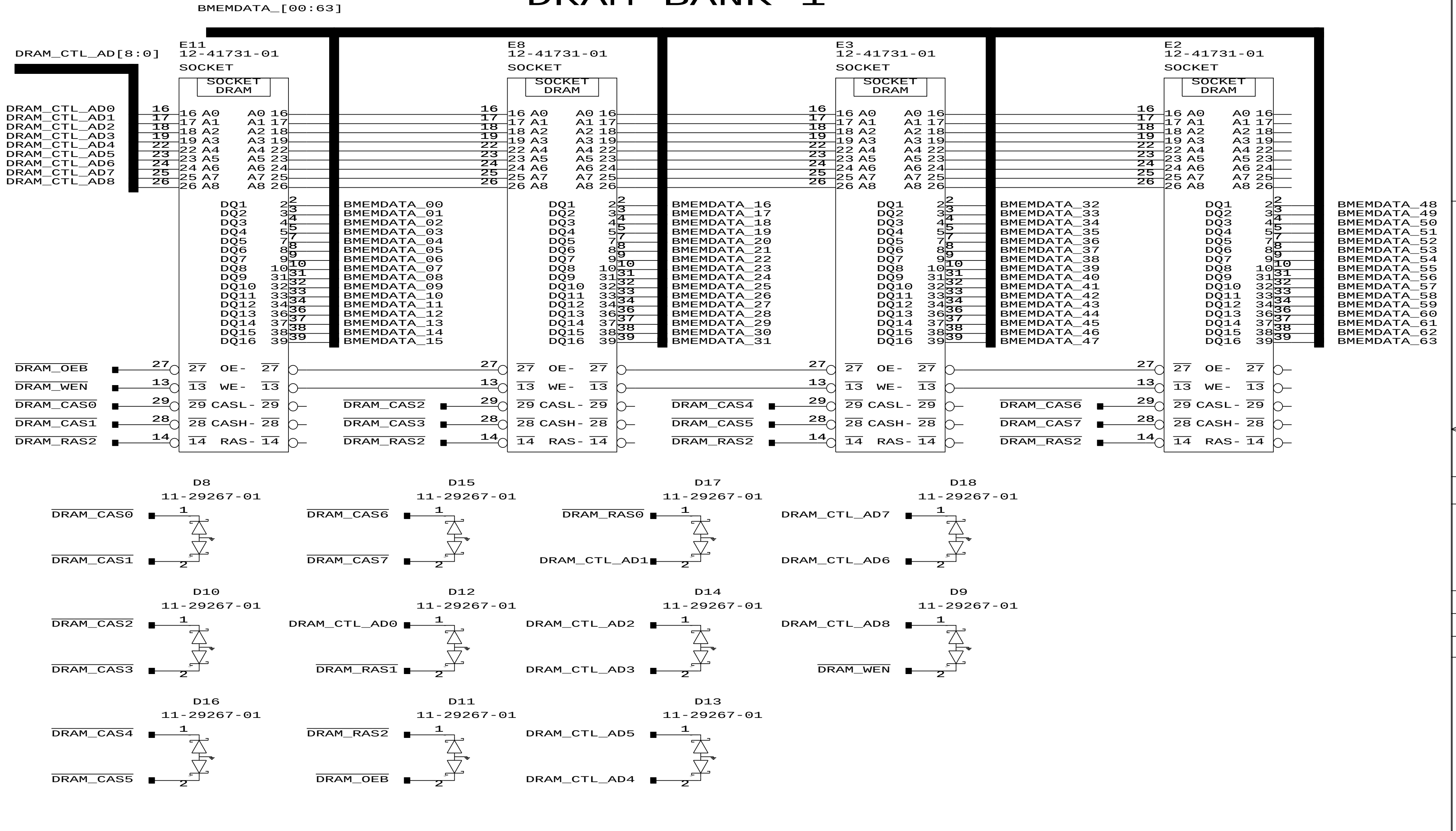
SIZE	CODE	NUMBER	REV.
B	CS	5424315-0-1	AX01

DRAM BANK 1



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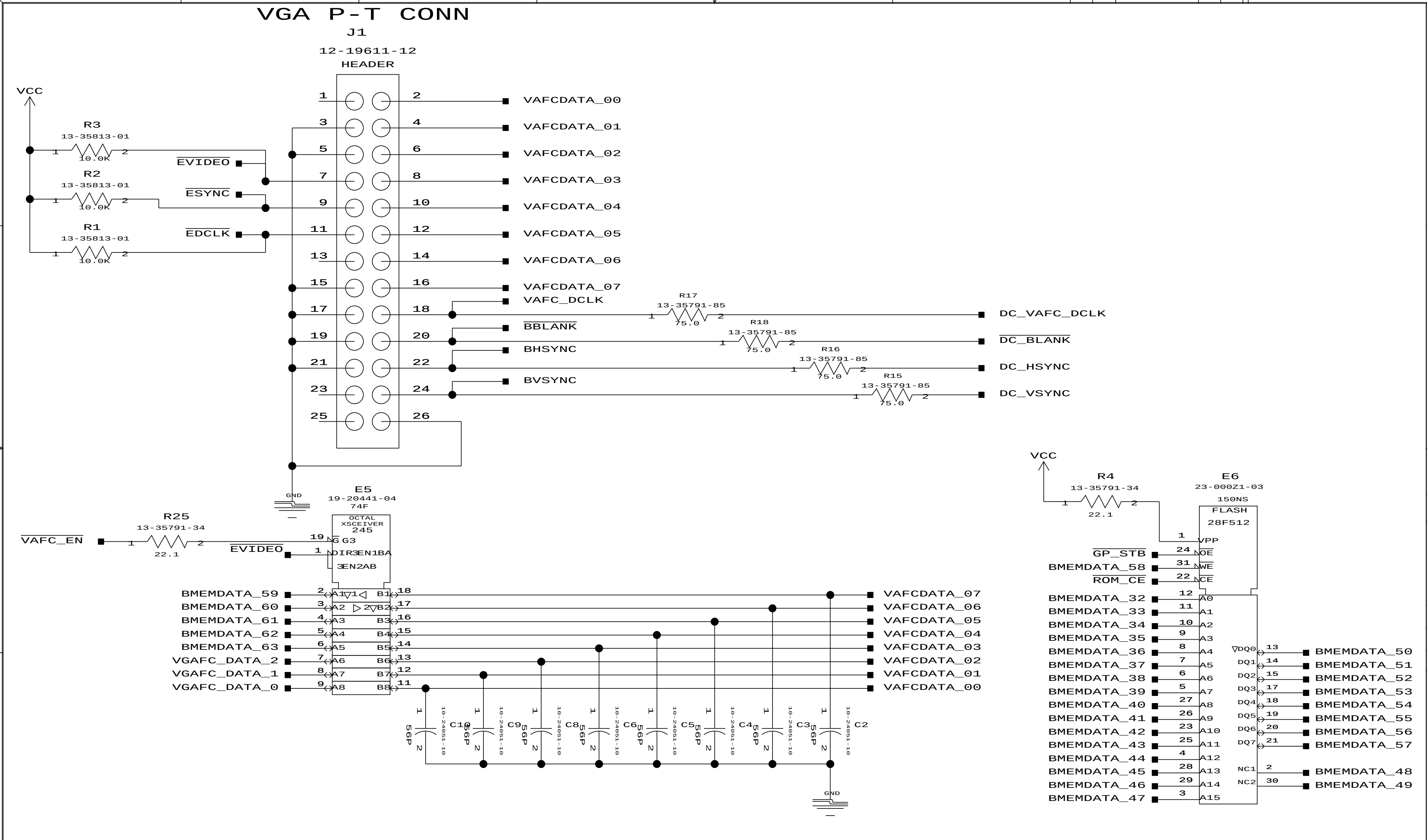
SHEET 5 OF 8
TOP DOCUMENT NUMBER: K-DD-5424315-0-0
TITLE: 21130 EVAL BOARD
SIZE B CODE CS NUMBER 5424315-0-1 REV. AX01



REVISION		
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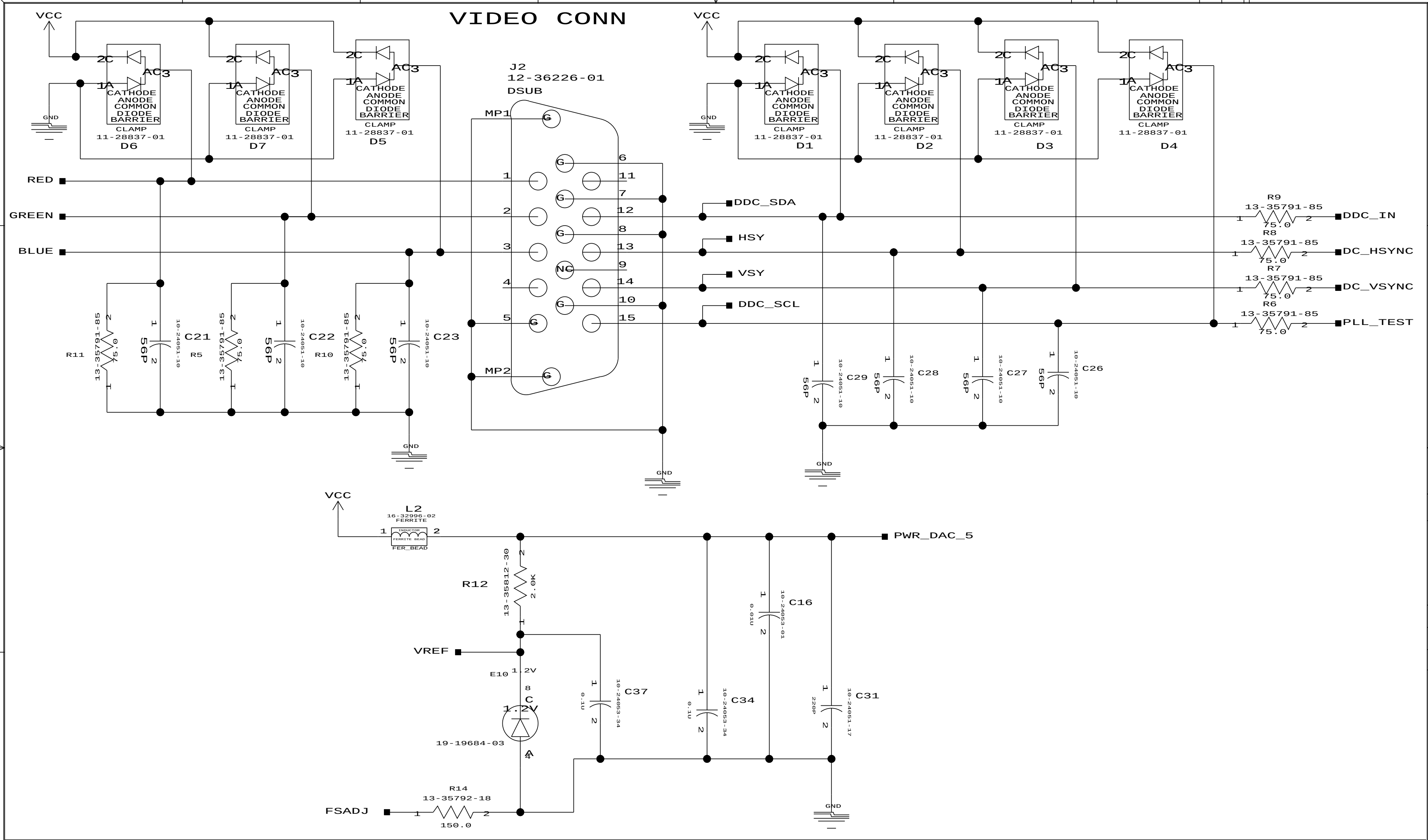
DRN. P. CAMPOS — DATE
CHK'D. — DATE
ENG. M. SULLIVAN — DATE
BOARD LOCATION:
SHEET 6 OF 8
USRA:
FIRST USED ON OPTION/MODEL:
TOP DOCUMENT NUMBER: K-DD-5424315-0-0

TITLE: 21130 EVAL BOARD

SIZE	CODE	NUMBER	REV.
B	CS	5424315-0-1	AX01

VIDEO CONN



REVISION		
CHK	CHANGE NO.	REV

digital

DRN. P. CAMPOS DATE
CHK'D. DATE
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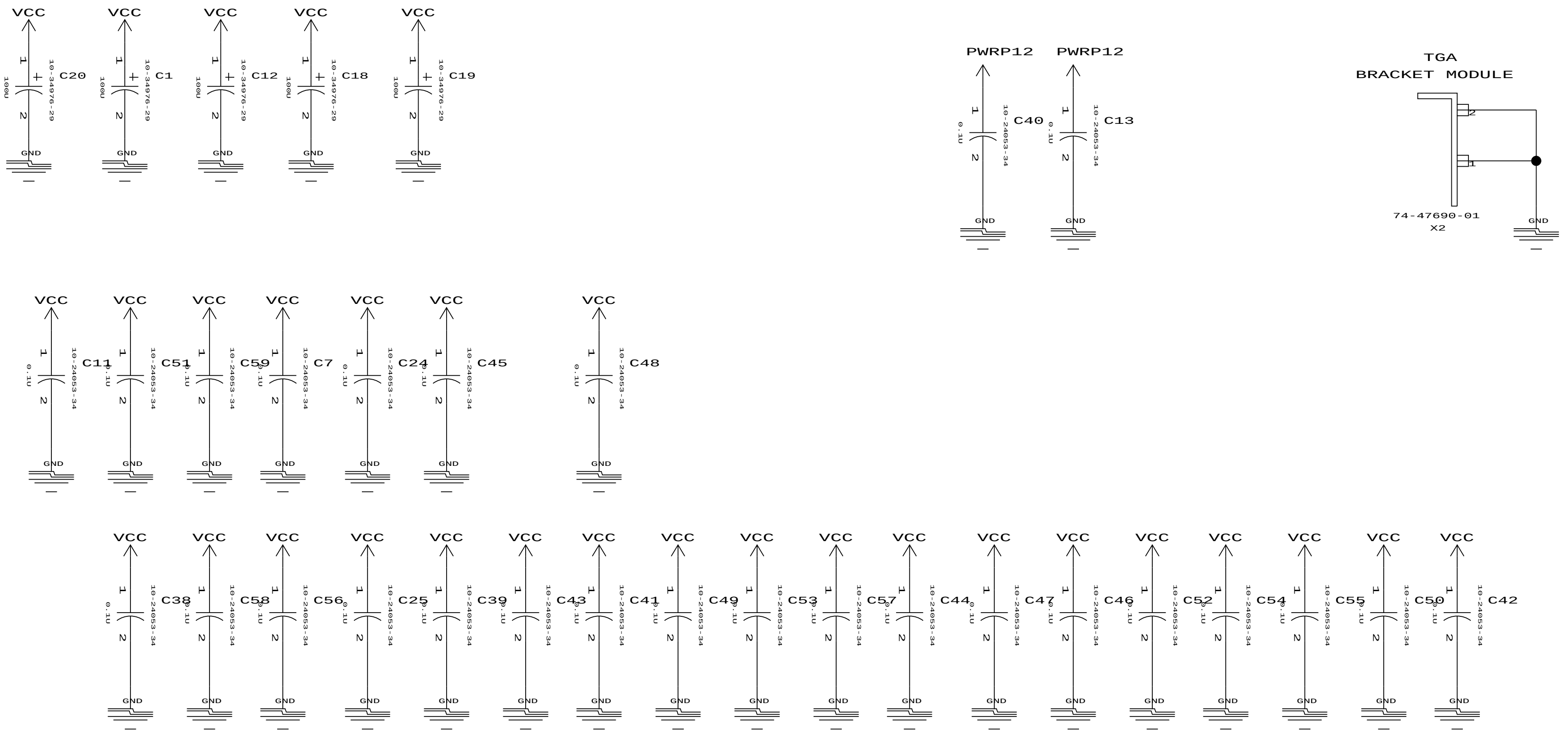
ENG. M. SULLIVAN DATE
BOARD LOCATION:
SHEET 7 OF 8
TOP DOCUMENT NUMBER: K-DD-5424315-0-0

TITLE: 21130 EVAL BOARD

SIZE	CODE	NUMBER	REV.
B	CS	5424315-0-1	AX01



REVISION		
CHK	CHANGE NO.	REV

digital

DRN. P. CAMPOS	DATE	ENG. M. SULLIVAN	DATE
CHK'D.	DATE	BOARD LOCATION:	
		SHEET 8 OF 8	
USRA:		TOP DOCUMENT NUMBER: K-DD-5424315-0-0	
FIRST USED ON OPTION/MODEL:			

TITLE: 21130 EVAL BOARD

SIZE	CODE	NUMBER	REV.
B	CS	5424315-0-1	AX01

SIZE D | CODE MD | NUMBER 5024314-0-0 | REV AX00

DATE	RESPONSIBLE ENGINEER	ECO NUMBER	REV

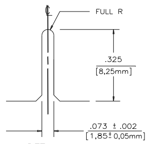
VIEWED FROM SIDE 1

PRINTED WIRE BOARD LAYER CONSTRUCTION

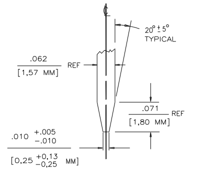
LAYER	DIELECTRIC SPACING		LAYER TYPE	COPPER WEIGHT	LINE WIDTHS
1			SIGNAL	0.5 OZ + PLATING	0.006 (0,15mm)
	0.015 +/- 0.0029	0,38mm +/- 0,073mm			
2			PLANE	1.0 OZ	
	0.020 REFERENCE	0,50mm REFERENCE			
3			PLANE	1.0 OZ	
	0.015 +/- 0.0029	0,38mm +/- 0,073mm			
4			SIGNAL	0.5 OZ + PLATING	0.006 (0,15mm)

OVERALL THICKNESS (PLATING-TO-PLATING): 0.062 +/-0.006 1,58mm +/-0,16mm.
OUTER LAYERS ARE STARTED WITH 0.5 OZ COPPER PLATED TO 0.0014 (0,035mm) MINIMUM COPPER THICKNESS.
0.5 OZ COPPER THICKNESS IS 0.0007 (0,017mm) NOMINAL 0.0003 (0,007mm) MINIMUM AFTER PROCESSING.
1.0 OZ COPPER THICKNESS IS 0.0014 (0,035mm) NOMINAL 0.0010 (0,025mm) MINIMUM AFTER PROCESSING.
TOLERANCES FOR LINEWIDTHS ABOVE IS +/- 0.0015 (0,036mm). FOR ALL OTHERS REFER TO DIGITAL STANDARD 176.

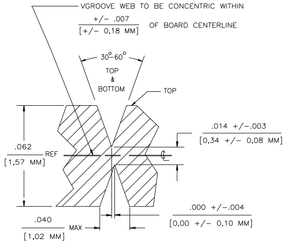
1. IF A CONFLICT BETWEEN THIS DOCUMENTATION/DESIGN PACKAGE AND ANY OTHER REFERENCED DOCUMENT EXISTS, THIS DOCUMENT /DESIGN PACKAGE WILL TAKE PRECEDENCE.
2. ALL ARTWORK FEATURES (IN ALL FORMATS) ARE SUPPLIED AT NOMINAL DIMENSIONS. UNLESS OTHERWISE SPECIFIED,THE FINISHED CIRCUIT SHOULD REFLECT THESE DIMENSIONS INCLUDING ALLOWABLE FABRICATION TOLERANCES PER DIGITAL STANDARD 176. ALL ARTWORK AND DRILL FEATURES MAY BE MODIFIED TO ACCOMODATE SPECIFIC FABRICATION PROCESSES.
3. ALL COPPER FOIL SHALL MEET OR EXCEED ANSI/IPC CF-150 TYPE ED (ELECTRODEPOSITED) CLASS I REQUIREMENTS.
4. DIELECTRIC MATERIAL TO BE FR4 WITH A MINIMUM GLASS TRANSITION TEMPERATURE OF 135 DEGREES C.
5. NICKEL AND GOLD PLATE FINGER SET AREA PER DIGITAL STANDARD 176. VENDOR TO ADD PLATING BUSS BAR.
6. DIGITAL-APPROVED LIQUID PHOTOIMAGABLE SOLDERMASK (LPSIM) IS REQUIRED ON BOTH SIDES OF THE PWB. FOR SURFACE MOUNT DEVICE PADS OF 50 MIL PITCH AND FINER, THE SOLDERMASK DATA DEFINES THE PAD SOLDERABLE SURFACE BY INTENTIONALLY PLACING SOLDERMASK OPENINGS DIRECTLY ON THE ETCH PAD SURFACE. FOR THESE DEVICES, THE SOLDERMASK ARTWORK FEATURES ARE SUPPLIED AT NOMINAL DIMENSIONS REFLECTING THE DESIRED SOLDERMASK DEFINED ETCH PAD SURFACE FOR THE FINISHED PRODUCT. ALL OTHER SOLDERABLE SURFACE ETCH FEATURES ARE SUPPLIED AT ZERO CLEARANCE TO ASSOCIATED ETCH FEATURES REFLECTING DESIRED COVERAGE.
7. ALL 0.015 (0.38mm) DIAMETER HOLES ARE TO BE DRILLED 0.015 (0.38mm) MINIMUM DIAMETER.
8. EACH CIRCUIT TO BE V-GROOVED AS INDICATED BY DASHED LINES, ONE (1) PLACE. REFER TO SECTION C-C FOR ADDITIONAL INFORMATION.
9. AREAS INDICATED BY CROSSHATCH ARE TO REMAIN ON THE PWB FOR THE MANUFACTURING ASSEMBLY PROCESS. THE PWB FABRICATOR SHALL COVER ALL CROSSHATCHED AREAS WITH SOLDERMASK ON BOTH SIDES OF THE PWB. THE PWB FABRICATOR MAY UTILIZE ALL CROSSHATCHED AREAS AS PART OF THEIR PWB PROCESS PANEL TOOLING AREA. PWB PROCESS FABRICATION FEATURES (IE:TOOLING HOLES,TEST/DRILL COUPONS;ETC.) ARE ACCEPTABLE IN CROSSHATCHED AREA.
10. THE PWB FABRICATOR IS REQUIRED TO ADD ONE (1) BREAKAWAY V-GROOVED TOOLING STRIP AS INDICATED BY THE CROSSHATCHED AREA ON THIS DRAWING. THE TOOLING STRIP IS TO HAVE TWO (2) 0.157"0.002" DIAMETER NPTH IN THE CORNER LOCATIONS MARKED "D".
11. EDGE BEVEL ACCEPTABLE ALONG ENTIRE BOTTOM EDGE OF THE CIRCUIT. SEE SECTION B-B.



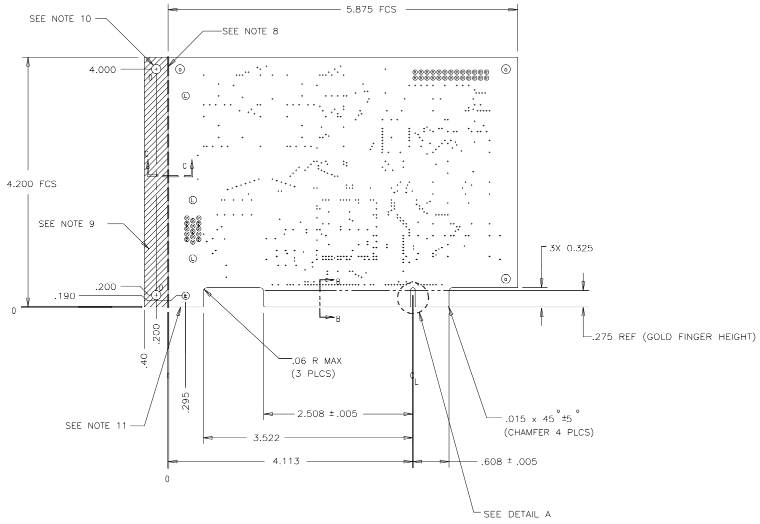
DETAIL A
SCALE: NONE



VIEW B-B
SCALE: NONE
2 PLACES



SECTION C-C
SCALE:NONE
ROTATED 90°



HOLE DATA (FOR STANDARD HOLE TOLERANCES USE DEC STD 176)				
SYMBOL	+	⊚	Ⓛ	⊙
FINISHED HOLE SIZE (INCHES)	.015	.040	.128	.157
POSITIVE TOLERANCE (INCHES)	.003			.002
NEGATIVE TOLERANCE (INCHES)	.015			.002
FINISHED HOLE SIZE (mm)				
POSITIVE TOLERANCE (mm)				
NEGATIVE TOLERANCE (mm)				
PLATED	Y	Y	Y	N
QUANTITY	544	41	4	3

FROM LAYER 1 TO LAYER 4

FABRICATION INFORMATION — MATERIAL AND WORKMANSHIP FOR ALL FABRICATED PRINTED WIRING BOARDS MUST MEET THE REQUIREMENTS OF DEC STD 176

FABRICATE BOARD PER: ____ AS SHOWN X | STEP AND REPEAT CODE: NONE | PRESS FIT COMPONENTS: YES ___ NO X

DESIGN INFORMATION

- NUMBER OF LAYERS: 4 LAYER CONSTRUCTION: ____ AS SHOWN X
- CONTROLLED IMPEDANCE: YES ___ NO X CONTROLLED CAPACITANCE: YES ___ NO X
- SURFACE MOUNT TECH / MINIMUM PITCH: SIDE 1 0,5mm SIDE 2 >.050
- PLANAR RESISTOR TECHNOLOGY: YES ___ NO X NUMBER OF PRT LAYERS ___
- BOARD FINISH: REFLOW TIN LEAD ___ HASL X ALL COPPER ___ OTHER ___
- SOLDERMASK: NONE ___ SIDE 1 X SIDE 2 X | SMOBC: YES X NO ___
- NOMENCLATURE: NONE ___ SIDE 1 X SIDE 2 X | TENTED VIAS: YES ___ NO X
- MINIMUM VIA HOLE SIZE: .015 MINIMUM COMPONENT HOLE SIZE: .040
- PAD EXPANSION: OUTER LAYERS X SIGNAL INNER LAYERS ___ NONE ___
- INCIRCUIT THIEVING: NONE ___ SIDE 1 X SIDE 2 X AS SHOWN ___
- TECHNOLOGY (LW/LS): LINE .006 SPACE .007
- CIRCUIT OUTLINE/FINGER DETAIL: ____ AS SHOWN X
- SPECIAL REQUIREMENTS: ____

TOLERANCES
INCHES UNLESS OTHERWISE SPECIFIED

INCHES		mm		ANGLES
.XXX	± .010	,XX	± ,25	±0 DEG
.XX	± .020	,X	± ,50	30 MIN
.X	± .100	X,	± 2,50	

APPROVALS	DATE
DRAWN: STEVE BAKER	27-FEB-95
CHECKED: DAVE DROZD	27-FEB-95
MECH ENG: PAUL CAMPOS	27-FEB-95
PROJ ENG: MIKE SULLIVAN	27-FEB-95
MFG ENG:	

SCALE: 1:1
SHEET 1 OF 1
TOP DOC NO: K-DD-5024314-0-0

digital™

TITLE:
CIRCUIT DRILL AND ETCH DRAWING

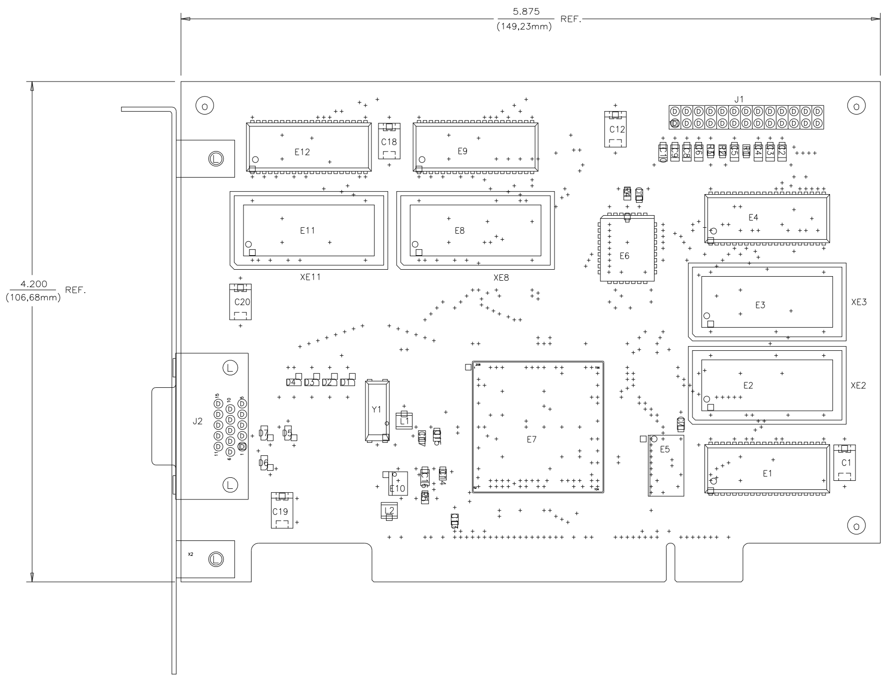
SIZE	CODE	NUMBER	REV
D	MD	5024314-0-0	AX00

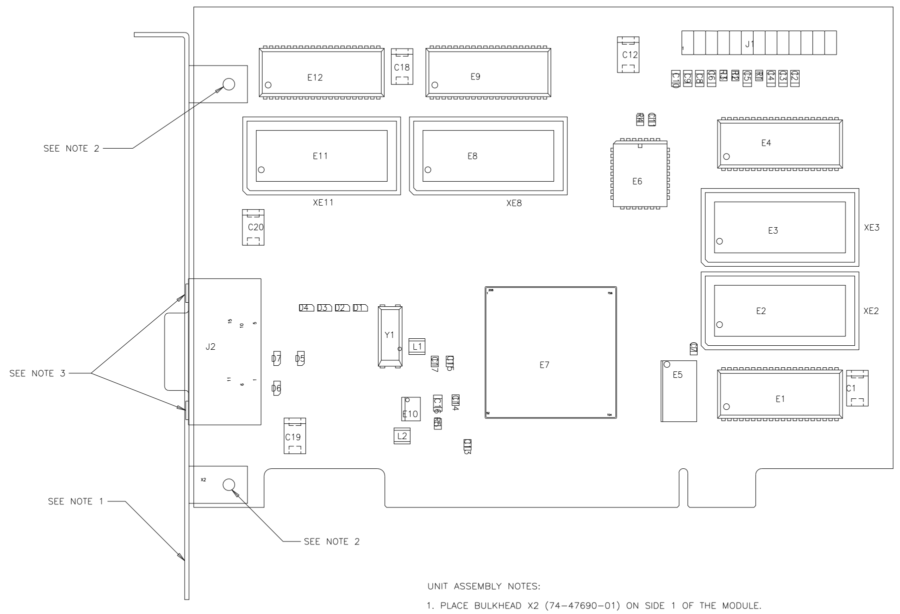
ETCH REV: A1 MEDIA K

WO# 298339

SIZE	CODE	NUMBER	REV
D	UA	5424315-0-0	AX00

VIEWED FROM SIDE 1





UNIT ASSEMBLY NOTES:

1. PLACE BULKHEAD X2 (74-47690-01) ON SIDE 1 OF THE MODULE.
2. FASTEN BULKHEAD X2 TO MODULE WITH 2 SCREWS (90-09643-02) FROM SIDE 2.
3. PLACE WASHERS (90-06688-00) ON TO STANDOFFS (90-00001-64) ONTO VIDEO CONNEVTOR J2 THROUGH BULKHEAD. TIGHTEN TO 3 in/lbs.
4. 74-47690-01 IS TO BE MODIFIED BY MIKE SULLIVAN OR PAUL CAMPOS BEFORE ASSEMBLY.
5. THERE ARE NO TESTPOINTS PER THE ENGINEER, MIKE SULLIVAN.

DATE	RESPONSIBLE ENGINEER	ECO NO	REV	DATE	RESPONSIBLE ENGINEER	ECO NO	REV

NOTES:

DESIGN INFORMATION

SURFACE MOUNT TECHNOLOGY: SIDE 1 X SIDE 2 X NONE ____

APPROVALS	DATE
DRAWN: STEVE BAKER	27-FEB-95
CHECKED: DAVE DROZD	27-FEB-95
MECH ENG: PAUL CAMPOS	27-FEB-95
PROJ ENG: MIKE SULLIVAN	27-FEB-95
MFG ENG:	
SCALE: 2:1	
SHEET 1 OF 3	
TOP DOC NO: K-DD-5424315-0-0	

digital™

TITLE: DAGGER EVAL BOARD

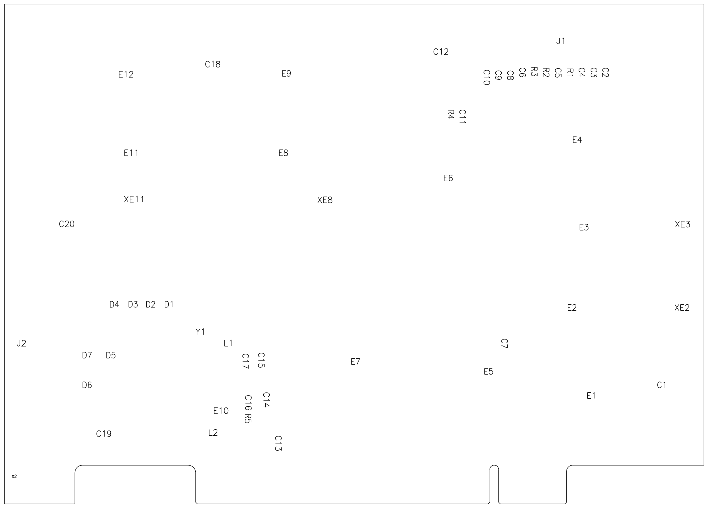
SIZE	CODE	NUMBER	REV
D	UA	5424315-0-0	AX00

ETCH REV A1 MEDIA K

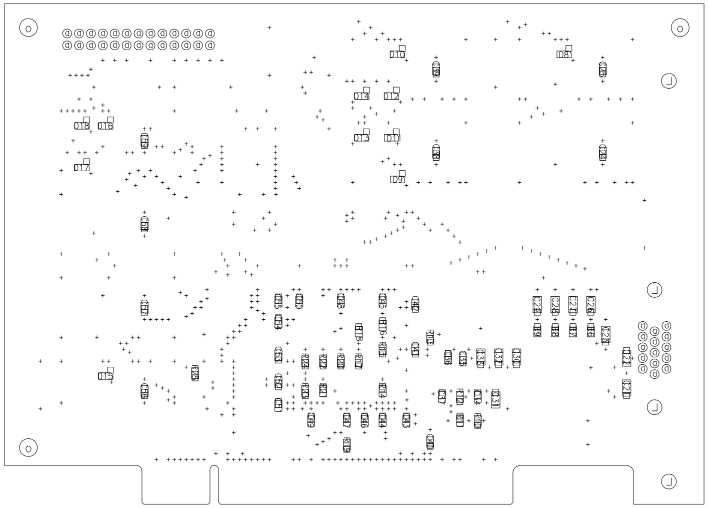
WO# 298339

SIZE D CODE UA NUMBER 5424315-0-0 REV AX00

VIEWED FROM SIDE 1



VIEWED FROM SIDE 2

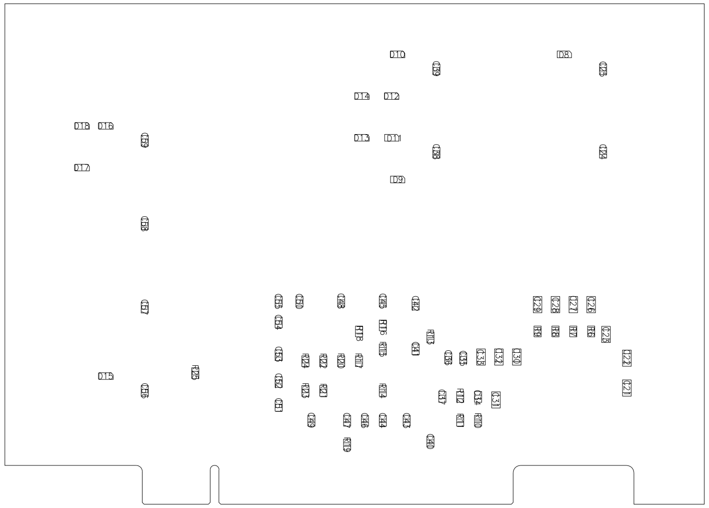


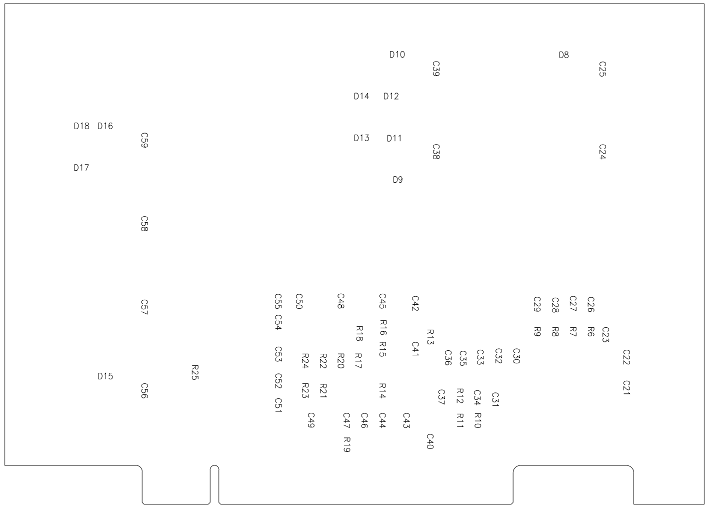
TITLE	DAGGER EVAL BOARD

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV
D	UA	5424315-0-0	AX00
SCALE 2:1		MEDIA K	SHEET 2 OF 3

WO# 298339

VIEWED FROM SIDE 2





TITLE	DAGGER EVAL BOARD

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV
D	UA	5424315-0-0	AX00
SCALE 2:1		MEDIA K	SHEET 3 OF 3

WO# 298339