1.0 Microprocessor Access

As seen on the microprocessor bus there are eight I/O addresses, selected by RS[2:0]. Two indirect schemes are used to access all of the internal registers and arrays through these eight primary I/O addresses.

The first scheme is standard VGA, and operates when RS[2] = 0. Of the four I/O addresses then available with RS[1:0], only one address directly accesses a register, the Pixel Mask. The other three addresses are used to indirectly access the three 256x8 palettes.

The second scheme is an indexed scheme and is used to access all of the remaining registers including the cursor array. This scheme operates when RS[2] =1. Of the four I/O addresses then available using RS[1:0], two are used to load an index register (Low and High). The third address is used to write or read the register or array position pointed to by the index register. The fourth address is used to directly access a register which controls whether the index register automatically increments following an indexed register access.

The eight I/O addresses selected by RS[2:0] are listed in Table 1 below:

Table 1. I/O Addresses

RS[2:0]	Register
000	Palette Address (Write Mode)
001	Palette Data
010	Pixel Mask
011	Palette Address (Read Mode)
100	Index Low
101	Index High
110	Index Data (Indexed Registers)
111	Index Control

1.1 VGA Access

1.1.1 Palette

Internally the three 256x8 palettes are accessed by the microprocessor as a single 256x24 palette, with all 24 bits written or read in one operation.

A single Palette Address register points to 1 of 256 locations for writing or reading the 24 bits. Two different Register Select addresses are used to access the Palette Address register.

A write to RS[2:0] = 000 (Palette Address Write Mode) initializes the palette logic for write operations. Subsequent writes to Palette Data (RS[2:0] = 001) will load internal palette color registers and cause these register contents to be written into the palettes.

A write to RS[2:0] = 011 (Palette Address Read Mode) initializes the palette logic for read operations. Data from the palettes will be loaded into internal palette color registers. Subsequent reads from Palette Data (RS[2:0] = 001) will read these palette color registers.

Every three accesses of Palette Data (RS[2:0] = 001) will cause the Palette Address register to be incremented. An increment past 0xff will "wrap around" to 0x00.

A read from either Palette Address (Write Mode) or Palette Address (Read Mode) will read the Palette Address register. The same register is used for writing and reading, thus, changing modes destroys the contents of the previous mode's palette address. For example, if some reads are performed and then Palette Address (Write mode) is written, the read address will be lost and a read of either Palette Address (Write Mode) or Palette Address (Read Mode) will produce the same result: the address that was written into Palette Address (Write Mode).

1.1.2 Palette Write

Palette writes must be initialized by writing the Palette Address (Write Mode) register. This provides a starting address for writes and initializes the internal circuitry for palette write operations.

Palette writes are then performed by writing to Palette Data in a red, green, blue... sequence. These writes will load internal palette data registers in sequence. Immediately following every third write, an internal write will be triggered to the palette of the 24 bits contained in the internal palette data registers, at the address contained in the Palette Address register.

Immediately following the internal palette write triggered by the third write to Palette Data, the Palette Address register will be incremented. Thus, continuous writes to Palette Data will load the palette, stepping through the palette addresses in ascending order.

1.1.3 Palette Read

Palette reads must be initialized by writing the Palette Address (Read Mode) register. This provides a starting address for reads and initializes the internal circuitry for palette read operations.

Immediately following the writing of Palette Address (Read Mode), a read of the palette will be performed at the address just written. Internal palette data registers are loaded with the read data, and the Palette Address register is incremented.

Palette reads are then performed by reading from Palette Data. Red, green, blue... data from the preloaded internal registers will be presented in sequence. Immediately following every third read, an internal read of the palette to the 24 bits contained in the internal registers will be performed at the address contained in the Palette Address register.

Immediately following the internal palette read triggered by the third read of Palette Data, the Palette Address register will be incremented. Thus, continuous reads of Palette Data will read the palette, stepping through the palette addresses in ascending order.

1.1.4 6/8 Bit Palette Access

The original VGA had 6-bit DACs and 6-bit palette entries, and the low order 6 bits from/to the microprocessor port were written/read into the palette.

For the RGB528A, the DACs and palette entries are 8 bits. For non-VGA emulation all 8 bits are used. To emulate 6-bit VGA operation the upper 6 bits of the palette hold the VGA 6-bit color and the two low order bits are set to 00. The COL RES bit (color resolution) of the Miscellaneous Control 2 register determines if the access is 6-bit or 8-bit.

The reset condition is to emulate VGA using the 6 low order microprocessor data bits. COL RES is set to 6 bits. In this mode, for writing, microprocessor bits [7:6] are discarded, bits [5:0] are shifted to bits [7:2], and bits [1:0] are set to 00 before being written into the internal data registers. For reading, the internal data register bits [7:2] are shifted to bits [5:0], and bits [7:6] are set to 00 before being presented on the microprocessor data signals.

If COL RES is set to 8 bits then all 8 bits from/to the microprocessor will be written to and read from the color palette registers.

Note that the 6-to-8 bit translation is only done between the microprocessor port and the internal data registers. Internally, on writes, all 8 bits of the internal registers are written to the palette, and on reads, the internal registers retain all 8 bits read from the palette. Thus, if the palette is loaded with 8-bit values with COL RES set to 8 bits, and then the palette is read with COL RES set to 6 bits, the internal palette color registers will still be loaded with the 8 bits that were written into the palette. But the data read on the microprocessor data lines will be 6 bits.

1.1.5 Palette Clocking

Palette accesses are synchronized internally with the pixel clock. On writes, the pixel values of the previous cycle are held and displayed during the write cycle. Both of these features minimize disturbance of displayed pixels when the palette is accessed (anti-sparkle).

The pixel clock (as selected by the PCLK SEL bits in Miscellaneous Control 2) must be running for palette access to be valid.

The timings for the microprocessor signals are specified in units of pixel clocks. These specifications are derived from the requirement for the pixel clock to be running for palette access, as well as to allow time for the Palette Accesses and Palette Address increments to occur internally following a palette access.

1.1.6 Palette Access Status

The original VGA logic had an override for read accesses of the Palette Address (Read Mode) register. Instead of reading the Palette Address register, a value was returned that indicates the status of the last palette access, write or read.

The reset condition of the RGB528A is to return the address value for a read of Palette Address (Read Mode). The VGA logic may be emulated by setting the RADR RFMT bit in Miscellaneous Control 1. This causes the status of the last palette access to be returned.

The value of the status returned is 0x00 if the last write to Palette Address was Write Mode, and 0x03 if the last write to Palette Address was Read Mode.

1.1.7 Pixel Mask

The pixel mask is an 8-bit register addressed with RS[2:0] = 010. It can be accessed at any time without disturbing a palette write or read sequence.

Accesses to the pixel mask are asynchronous to the pixel clock. Temporary color disturbances can be expected if the mask is changed while displaying pixels through the palette.

1.2 Indexed Access

The cursor array and a number of control registers are addressed with an internal 11-bit index register. The microprocessor accesses this as Index High (RS[2:0] = 101) and Index Low (RS[2:0] = 100).

A write or read to Index Data (RS[2:0] = 110) actually writes or reads the register/cursor array location addressed by the Index register.

Following a write or read of Index Data, the index register will increment if the INDX CNTL bit is set. The Index Control register (RS[2:0] = 111) contains this bit. To allow for future expansion, wraparound from 0x07ff to 0x0000 is **not** supported.

In general, access of Index Low, Index High, Index Control, or any of the Indexed registers is independent of the palette access and will not disturb a palette write or read sequence. However, as described above the PADR RFMT bit in Miscellaneous Control 1, the COL RES bit in Miscellaneous Control 2, and the 6BIT ACC bit in Palette Control all affect palette access.

Also, as described above, the pixel clock must be running for valid access of the palette, and the pixel clock is affected by a number of indexed registers.

1.2.1 Cursor Array

In general, the indexed registers may be written or read at any time, using the address held in Index High and Index Low. This address may be set by writing to Index High or Index Low, or the value may result from the auto-increment action of a previous access.

However, as described in 5.2.3, "Cursor Array Reads," on page 23, to access the cursor array a write to Index High or Index Low must be performed first. That is, the cursor array cannot be accessed by auto-increment from address 0x00ff to 0x0100.

Also, as with the palette, the pixel clock must be running to access the cursor array.

2.0 Clocking

2.1 Clock Generators

There are two on-board clock generators: pixel clock and system clock (SYSCLK). Each clock generator uses a separate programmable phase locked loop (PLL).

The pixel clock generator provides the fundamental "dot" timings; it serves generally as the clock both for internal chip clocking and for on-card CRT timings.

The system clock generator is provided for the convenience of the graphics subsystem design. No internal use is made of this clock; the clock generator simply drives the SYSCLK output of the chip.

2.2 PLL Input

2.2.1 REFCLK

The REFCLK input is a reference clock that the PLLs use in conjunction with programming registers to produce a wide variety of frequencies.

In general, REFCLK can be any frequency from 2 MHz through 100 MHz.

As discussed below, following a reset the PLL driving the SYSCLK output is enabled with the startup frequency:

SYSCLK frequency = (33/16) × REFCLK frequency

If it is important to have a particular frequency on SYSCLK following a reset, then the REFCLK frequency must be chosen that produces the desired SYSCLK frequency.

Also, when the "direct programming" method is used to program the PLL frequencies (see below), then REFCLK must lie on a 2 MHz boundary in the range of 4 MHz through 62 MHz (4 MHz, 6 MHz, 8 MHz,... 62 MHz).

2.3 SYSCLK PLL Output

The system clock PLL drives the SYSCLK output. Two bits in the System Clock Control register affect this output. Bit 6, SYSC DSAB, is used to 3-state the driver. Bit 1, SYSC SRC, is used to bypass the SYSCLK PLL (the incoming REFCLK is steered to the SYSCLK output).

The supported frequency range for SYSCLK is 16.25 MHz to 100 MHz.

2.4 Pixel PLL Outputs

The pixel PLL is used internally as the pixel clock. The maximum allowed generated frequency is 170/220/250 MHz, dependent on the product version.

The pixel PLL Output is not available directly. However, two divided versions are provided as output signals:

- SCLK
- DDOTCLK

2.5 SCLK

SCLK (Serial Clock) is intended for clocking of the serial outputs of the VRAMs to the pixel port inputs. As such, the divide factor is a function of the VRAM pixel port width (128, 64 or 32 bits), and the number of pixels contained in an access. For example, with a VRAM width of 64 and operating at 16 bits-per-pixel, there will be 64/16 = 4 pixels brought in with each VRAM access, and SCLK will operate at 1/4 the frequency of the pixel PLL output.

If the VGA port is selected SCLK will simply be the output of the pixel PLL. Table 2, "SCLK Frequencies," is a table of all the SCLK frequencies that are produced.

"24 Packed" is a special case. It is not valid with a VRAM width of 32. For a VRAM width of 64 it produces 3 SCLKs for every 8 internal pixel clocks, and for a VRAM width of 128 it produces 3 SCLKs for every 16 internal pixel clocks, as shown in Figure 1.

The double buffer modes also affect the SCLK timing (see 3.6, "Double Buffer Modes," on page 17). The "Dual 64 Bit Buffer mode", with a VRAM width of 128, selects only half the bits, and so runs the SCLK at the same frequency as normally used for a VRAM width of 64. The "8 BPP Double Buffer" mode works on 16 bit boundaries, and so runs SCLK as if the pixel format was 15/16 BPP.

The SCLK output can be inverted with the SCLK INVT bit of the Miscellaneous Clock Control register. This allows either polarity to be used, as desired, to aid in meeting critical timings at the card level.

Table 2. SCLK Frequencies

BPP	VRAM=32	VRAM=64	VRAM=128	VRAM=64, Dual 64 Bit Buffer
4	÷8	÷ 16	Invalid	÷ 16
8	÷4	÷	÷ 16	÷
15/16	÷	÷ 4	÷ 8	÷ 4
32	÷1	÷ 2	÷ 4	÷ 2
24 Packed	Invalid	÷ (8/3)	÷ (16/3)	÷ (8/3)
8 BPP Dbl Buf	÷2	÷	÷8	Not Applicable
VGA	÷ 1			

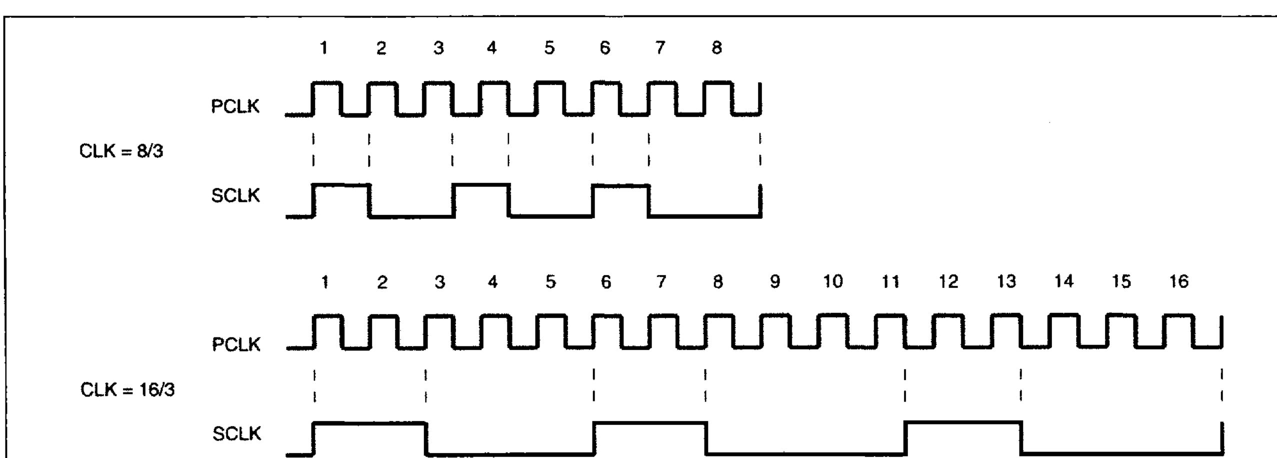


Figure 1. SCLK for 24 BPP Packed

The SCLK DSAB bit of the Miscellaneous Clock Control register can be used to 3-state the SCLK output if desired.

2.5.1 DDOTCLK

DDOTCLK (Divided Dot Clock) is simply the pixel PLL output divided by 1, 2, 4, 8 or 16 as determined by the DDOT DIV bits of the Miscellaneous Clock Control register.

Note that the maximum supported output frequency of DDOTCLK is 100 MHz, so some values of the DDOT DIV bits will become illegal when the pixel PLL is programmed to operate beyond this frequency.

When a pixel format of 24 BPP Packed is selected, the SCLK output may be driven on DDOTCLK instead of the divided pixel PLL output, under control of the B24P DDOT bit of the Miscellaneous Clock Control register.

DDOTCLK is similar to the SYSCLK output in that it is provided for general card use and is not used internally. However, its frequency is slaved to the pixel clock, whereas SYSCLK is independent. The DDOTCLK may be 3-stated with the DDOT DSAB bit of the Miscellaneous Clock Control register if desired.

Note: Although DDOTCLK and SCLK are both derived from the pixel clock, there is otherwise no particular relationship between the two clocks. In particular, the two clocks do not have any associated phase relationship.

2.6 Additional Clocks

2.6.1 Load Clock

The LCLK input (Load Clock) is used to latch up all incoming pixel data and video controls. The maximum frequency of this input is 100 MHz.

2.6.2 Pixel Clock (Dot Clock)

The pixel clock, or dot clock, is the internal clock used to clock pixel data up through the DACs. It is also required to be running to access the palette and the cursor. The maximum frequency of this clock is 170/220/250 MHz (depending on the chip version).

There are several sources of the pixel clock, as selected by the PCLK SEL bits in the Miscellaneous Control 2 register:

LCLK input This is the reset default. It is intended to be used when the VGA port is selected as the pixel source.

Pixel PLL output This is intended to be used when the VRAM pixel port is selected as the pixel source. It provides the highest pixel clock operation.

REFCLK input This is intended for laboratory bringup.

When LCLK is selected as the pixel clock all internal pixel operations are synchronous with LCLK. If the pixel clock is sourced by the pixel PLL output or REFCLK, then the incoming pixels and video controls are expected to be derived from SCLK. After latching the signals with LCLK, the signals are clocked with an internal SCLK, and then clocked with the internal pixel clock. LCLK must maintain a specified relationship to SCLK to achieve the internal transfer of the clocking from LCLK to SCLK.

2.7 PLL Setup and Reset

2.7.1 Pixel PLL

The PLL is enabled for running at a programmed frequency by setting the REF DIV COUNT, VCO DIV COUNT, and DF bits (as described in the following sections), and then setting the PLL ENAB bit of the Miscellaneous Clock Control register.

When the PLL ENAB bit is 0 (off), the PLL will continue to run but the frequency will not be determined by programming values. The PLL will drive to its lowest frequency of operation, in the range of 5 KHz to 250 KHz.

The pixel clock frequency is determined by the DF programming bits. When DF = 00, the pixel clock is equal to the PLL clock divided by 4 (1.25 KHz to 62.5 KHz). When DF = 01 the pixel clock equals the PLL clock divided by 2 (2.25 KHz to 125 KHz), and when DF = 10 or 11, the pixel clocks equals the PLL clock (5 KHz to 250 KHz.)

Following a reset, the PLL ENAB bit is off and the DF bits of all programming registers are set to 00, so the pixel clock will be PLL clock/4 = 1.25 KHz to 64.25 KHz.) The PORT SEL bit of Miscellaneous Control 2 register will be 0 (VGA port), which will cause the SCLK output to be the same as the pixel clock (1.25 KHz to 64.25 KHz.) The DDOT DIV bits of the Miscellaneous Clock Control register will be zero, which will cause DDOTCLK to also be the same frequency as the pixel clock.

2.7.2 SYSCLK PLL

The SYSCLK PLL is enabled with the SPLL ENAB bit of the System Clock Control register. Unlike the pixel PLL, following a reset, this ENAB bit will be set, and the SYSCLK PLL will be running and driving the SYSCLK driver. The output frequency will be (33/16) × REFCLK.

When the SPLL bit is 0 (disabled) the SYSCLK PLL will run in the 5 KHz to 250 KHz range similar to the pixel PLL. The frequency driven on the SYSCLK output will be determined by the value of the DF bits in the System PLL VCO Divider register), using the same divide factors as described above for the pixel PLL.

Table 3. PLL Equations

DF	Output Frequency	Internal VRF	Max Output Freq. (MHz)		
			170	220	250
00	$\frac{\text{FREF} \times (\text{VCO DIV COUNT} + 65)}{(\text{REF DIV COUNT}) \times 8}$	$\frac{\text{FREF}}{(\text{REF DIV COUNT}) \times 2}$	42.5	55.0	62.5
01	$\frac{\text{FREF} \times (\text{VCO DIV COUNT} + 65)}{(\text{REF DIV COUNT}) \times 4}$	$\frac{\text{FREF}}{(\text{REF DIV COUNT}) \times 2}$	85	110 (*)	125 (*)
10	$\frac{\text{FREF} \times (\text{VCO DIV COUNT} + 65)}{(\text{REF DIV COUNT}) \times 2}$	$\frac{\text{FREF}}{(\text{REF DIV COUNT}) \times 2}$	170 (*)	220 (*)	250 (*)
11	$\frac{\text{FREF} \times (\text{VCO DIV COUNT} + 65)}{\text{REF DIV COUNT}}$	$\frac{\text{FREF}}{\text{REF DIV COUNT}}$	170 (*)	220 (*)	250 (*)

1. FREF = REFCLK frequency
2. Frequencies marked with (*) are maximum pixel PLL frequencies. The SYSCLK PLL maximum output frequency is 100 MHz.

2.8 PLL Programming

The two PLLs are programmed identically. Three values are used:

REF DIV COUNT (Reference Divide Count) This number provides a count value for dividing down the incoming REFCLK. It must be between 2 and 31. Operation of the PLL is indeterminate if this number is 0 or 1.

VCO DIV COUNT (VCO Divide Count) This number provides a count value for the divider in the PLL feedback loop. The value can range from 0 through 63. Internally, 65 is added to VCO DIV COUNT, so that the PLL feedback divider value ranges from 65 through 128.

DF (Desired Frequency) These are two bits with values of 00, 01, 10, and 11. The intent of these bits is to divide the operation of the PLL into four frequency ranges. Following the divide of the REFCLK provided by the REF DIV COUNT there is an additional divide-by-two which is selected or bypassed with the DF bits. Also, the output of the PLL has a divider stage, or postscaler, that is controlled by the DF bits.

Table 3, "PLL Equations," gives the general formulas for programming the PLLs. Because of the action of the DF bits there are four equations, one for each DF bit setting.

It is possible to program the PLLs with values that generate illegal operating conditions:

1. The reference frequency VRF (Video Reference Frequency), which is internal to the PLL, cannot be less than 1 MHz.
2. The internal VCO (Voltage Controlled Oscillator) cannot exceed the rated speed of the product (170/220/250 MHz).
3. The SYSCLK output driven by the SYSCLK PLL cannot exceed 100 MHz.
4. The DDOTCLK output driven by the pixel PLL cannot exceed 100 MHz.

Table 3, "PLL Equations," gives the equations for calculating the internal VRF. Table 3 also gives the maximum allowable output frequency for each setting of DF. This reflects the action of the VCO postscaler. If the PLLs are programmed so that these maximum dot clock frequencies are not exceeded then the maximum VCO frequency will not be exceeded.

2.9 PLL Frequency Selection

The REF DIV COUNT, VCO DIV COUNT, and DF bits are provided to the PLLs in a pair of 8-bit registers. REF DIV COUNT is 5 bits and occupies one register, with the 3 high order bits unused. The 6 VCO DIV COUNT bits occupy the second register, with the 2 high order bits used by DF.

For the SYSCLK PLL, the two programming registers are the System PLL Reference Frequency, which holds REF DIV COUNT, and the System PLL VCO Divider, which holds VCO DIV COUNT and the DF bits.

For the pixel PLL, there are actually 17 registers which can be used to hold the programming values: Fixed Pixel PLL Reference Divider and F0 - F15. A pair of registers is selected from this group to provide the pixel PLL programming values. This selection is controlled by the pixel PLL Control 1 and pixel PLL Control 2 registers.

Two different programming styles are supported:

Direct Programming In this scheme only the register holding VCO DIV COUNT and DF is altered to change the frequencies. The register for REF DIV COUNT holds a value that is constant for all frequencies. This method is discussed in more detail below.

M over N In this scheme both register values are changed to program a new frequency. The name refers to the general PLL concept in which

Output frequency = Input reference × (M/N)

where VCO DIV COUNT serves as M and REF DIV COUNT serves as N, with modifications to the equation as shown in Table 3, "PLL Equations."

For the SYSCLK PLL there is not much distinction between the two programming styles. Both registers are written to provide an initial operating frequency. Then to change frequency either one register is changed (System PLL VCO Divider), or both registers are changed, depending on the programming style.

For the pixel PLL, a set of preprogrammed frequencies can be stored in the F0 - F15 registers, and the number of stored frequencies depends on the programming style.

When the direct programming style is used a single REF DIV COUNT is stored in the Fixed PLL Reference Divider register. Up to 16 values of VCO DIV COUNT and DF can be stored in the F0 - F15 registers, allowing 16 preprogrammed pixel clock frequencies.

With the M/N style the Fixed Pixel PLL Reference Divider register is not used. The F0 - F15 are reconfigured as 8 pairs of M and N values (M0,N0,M1,N1, ... M7,N7). This allows 8 preprogrammed pixel clock frequencies.

The selection of the programming registers, either 1 of the 16 F0 - F15 registers or 1 of the 8 M/N pairs, is done either externally with the FS[1:0] inputs to the module, or internally with the INT FS[3:0] bits of Pixel PLL Control 2 register. When the M/N style is used INT FS[3] is ignored.

The programming style and selection source is chosen with the EXT/INT bits of the Pixel PLL Control 1 register, as shown in Table 4, "Pixel PLL Control 1 EXT/INT Freq. Selection."

Table 4. Pixel PLL Control 1 EXT/INT Freq. Selection

EXT /INT	Frequency Selection	REF DIV COUNT	VCO DIV COUNT, DF
000	External FS[1:0]	Fixed Reference Divider	F0-F3
001	External FS[1:0]	N0-N3	M0-M3
010	Internal FS[3:0]	Fixed Reference Divider	F0-F15
011	Internal FS[2:0]	N0-N7	M0-M7

Note that there are more selections available with the internal register INT FS[3:0] than using the external FS[1:0] inputs. With the external inputs, only 4 frequencies can be chosen, using either direct programming or M/N. With the INT FS[3:0] bits 8 frequencies can be chosen using M/N or 16 frequencies can be chosen using direct programming.

Table 5. Direct Programming Reference Divider Values

REFCLK (MHz)	Fixed PLL Reference Divider Register Value
4	0x0002
6	0x0003
8	0x0004
10	0x0005
12	0x0006
14	0x0007
16	0x0008
18	0x0009
20	0x000a
22	0x000b
24	0x000c
26	0x000d
28	0x000e
30	0x000f
32	0x0010
34	0x0011
36	0x0012
38	0x0013
40	0x0014
42	0x0015
44	0x0016
46	0x0017
48	0x0018
50	0x0019
52	0x001a
54	0x001b
56	0x001c
58	0x001d
60	0x001e
62	0x001f

2.10 Direct Programming

Use the following steps to calculate the values used with direct programming:

1. Look up the REFCLK frequency in Table 5, "Direct Programming Reference Divider Values," and write the given programming value into the PLL Reference Divider register (System PLL Reference Divider for the SYSCLK PLL, Fixed Pixel PLL Reference Divider for the pixel PLL). If the incoming REFCLK frequency does not appear in this table, then the direct programming method cannot be used.
2. Use Table 6, "PLL Direct Programming Equations," to determine the values to write into the VCO Divider register (System PLL VCO Divider for the SYSCLK PLL, F0 - F15 for the pixel PLL). First, pick the row of the table whose frequency range covers the frequency of interest. This will determine the value of the DF bits to write. Next, use the given equation to calculate the value of the VCO DIV BITS. Write these two values together to the appropriate register.

   The generated pixel clock frequency is designated in this table as VF, for Video Frequency. Note that within each range the desired VF frequency must lie on a given step value (e.g., with DF = 11 a frequency of 159 MHz is invalid because it does not lie on a 2 MHz step; but either 158 MHz or 160 MHz is valid).

Table 6. PLL Direct Programming Equations

DF	VCO Divide Count	Frequency Range	Step (MHz)
00	(4 x VF) - 65	16.25 - 32 MHz	0.25
01	(2 x VF) - 65	32.5 - 64 MHz	0.5
10	VF - 65	65.0 - 128 MHz	1.0
11	(VF / 2) - 65	130.0 - 250 MHz	2.0
VF = Desired Video Frequency			

2.11 M/N Programming

For the "M over N" programming style use Table 3, "PLL Equations," in the following steps:

1. Select values for REF DIV COUNT, VCO DIV COUNT, and DF that generate the desired frequency (or come close enough). Note that the values 0 and 1 are illegal for REF DIV COUNT under all conditions.
2. Calculate the internal reference frequency VRF. Verify that this frequency is not less than 1 MHz.
3. Verify that the dot clock frequency does not exceed the maximum value specified in the table.
4. If conditions 2 and 3 are not met then the selected values cannot be used.

2.12 General PLL Programming

Fundamentally the only differences between the two programming styles are these:

1. Direct programming can be used only if the REFCLK frequency falls on a 2 MHz boundary from 4 MHz through 62 MHz.
2. With direct programming, for a given pixel clock frequency there is only one set of programming values. These values are obtained from Table 5, "Direct Programming Reference Divider Values," and Table 6, "PLL Direct Programming Equations." Illegal conditions cannot be generated as long as the correct value from Table 5, "Direct Programming Reference Divider Values," is used.
3. M/N can be used with any REFCLK frequency from 2 MHz through 100 MHz.
4. A given pixel clock can be generated with multiple combinations of programming values. Some of these values can produce illegal internal conditions. Table 3, "PLL Equations," is used to calculate the resulting pixel clock and to determine if conditions are violated.

If the incoming REFCLK does not meet the requirements for direct programming, then M/N programming must be used for both PLLs.

If REFCLK is suitable for direct programming, then the programming style for the SYSCLK PLL is generally a matter of convenience.

For the pixel PLL, the use of preprogrammed frequencies, and the number required, 8 or 16, can affect the choice of programming styles.

However, the register selection specified with the EXT/INT bits of the Pixel PLL Control 1 register does not necessarily force the selection of programming style, direct or M/N. For example, there is nothing to prevent an arbitrary value from being written into the Fixed Pixel PLL Reference Divider and writing an appropriate value into one of the F0 - F15 registers as calculated with the M/N method. Of course, if multiple "N" values are used and they have to be re-written to the Fixed Pixel PLL Reference Divider every time the FS[3:0] value changes, this defeats the purpose of the FS[3:0] selection mechanism.

Likewise, when the 1-of-8 M/N register selection is used there is nothing to prevent using the direct programming equations from being used for the values. The same value will wind up being used for all of the "N" values.

2.13 PLL Interaction

The Pixel PLL and the SYSCLK PLL will interfere with each other (they will modulate the output frequency of the other PLL) if the higher frequency falls within 3 MHz of an integer multiple of the lower frequency. That is, if f_{higher} is the higher of the two frequencies and f_{lower} is the lower frequency, then the following equation must be satisfied:

$$f_{higher} \neq (n \times f_{lower}) \pm 3\text{ MHz};\ n = 1,2,3\ldots$$

2.14 Glitching on Frequency Change

When the operating frequency of either PLL is changed by changing one of the programming register values, the transition from the original frequency to the new frequency can either occur smoothly or can glitch, depending upon the following:

1. If the DF bits are not changed, then changing the REF DIV COUNT and VCO DIV COUNT bits will not cause a glitch.
2. If the DF bits are changed, then the PLL output can glitch.

2.15 Diagnostic Readback

The read-only registers Pixel PLL VCO Divider Input and Pixel PLL Reference Divider Input contain the programming values actually used by the pixel PLL. These registers can be used to verify that the desired programming registers are the ones actually selected.

3.0 Modes of Operation

Pixel data can come from the VGA port or the VRAM pixel port, as selected by the PORT SEL bit of the Miscellaneous Control 2 register.

If the VRAM pixel port is selected, the pixel format can be 4 BPP (bits per pixel), 8 BPP, 15/16 BPP, 24 BPP Packed, or 32 BPP, selected by the Format bits of the Pixel Format register. Table 7, "Pixel Format Table," on page 18 shows how the input bits are selected as a function of Pixel Format.

VGA data and 4 BPP data are always used to indirectly generate 24 bits of color by indexing into the 256 entry palettes. The Pixel Mask register is used to selectively mask off the index bits as desired.

8 BPP, 15/16 BPP, 24 BPP Packed, and 32 BPP from the VRAM pixel port can either be indirect (through the palettes) or direct (bypassing the palettes).

Each of these formats has an associated control register with bits to select indirect or direct color. Additionally 15/16 BPP and 32 BPP formats allow a bit within the incoming data to dynamically select indirect or direct color.

As with VGA and 4 BPP, the Pixel Mask is used to mask off palette address bits with indirect color access for 8, 15/16, 24 Packed, and 32 BPP.

When the VRAM port is selected two "double buffer" modes are also available (see 3.6, "Double Buffer Modes," on page 17). In these modes for every two pixels clocked in only one is used - the other is discarded. The selection of one pixel or the other is under register control. These modes are for use when two independent images are constructed in the frame buffer, and it is desired to switch rapidly from one to the other.

All pixel formats are available with all VRAM widths, with these exceptions:

1. 24 BPP Packed is not available with a VRAM width of 32.
2. 4 BPP is not available with a VRAM width of 128. (However, in "64-Bit Double Buffer Mode" which uses a VRAM width of 128, 4 BPP is available.)

3.1 Pin Sharing

3.1.1 VGA Data

The eight VGA data inputs are shared with the VRAM data inputs PIX[127:120]. Thus for applications that use both the VGA input and all 128 VRAM inputs, there must be a mechanism at the card level for 3-stating one set of inputs while the others are active.

The VGAMODE output is available for this purpose. This output is simply the inverted state of the PORT SEL (Port Select) bit of the Miscellaneous Control 2 register. E.g., when this bit is set to 0 (VGA port selected), the VGAMODE output will be active (high).

3.1.2 Digital Output Data

The internal digital data bits just before the DACs, along with synchronized Blank and Clock signals, are made available as outputs (for driving flat panel displays - see 7.0, "Digital Outputs," on page 27). These outputs are shared with the VRAM inputs PIX[89:64].

Applications that use these digital outputs will not be able to use the upper 64 VRAM inputs at the same time, and thus will be restricted to a VRAM width of 64 or 32 bits.

3.2 Bit Ordering

Bit order is high-to-low. For 8 BPP, the MSB is '7' and the LSB is '0'; for 16 BPP the MSB is '15' and the LSB is '0', and so on.

When the VRAM pixel port is selected the default condition is to access the pixels from low to high. For each LCLK, the first pixel used is at the end with bit PIX[00], and the last pixel used is at the end with bit PIX[127] (bit PIX[63] for VRAM width = 64 and PIX[31] for VRAM width = 32). For example, for 8 BPP, the first pixel is PIX[07:00], the second pixel is PIX[15:08], and so on.

For a VRAM width of 128, the SWAP DWRD bit of the Miscellaneous Control 3 register may be used to swap the access order of the two incoming double words. When swapped, PIX[127:64] will be used for the first pixel(s) and PIX[63:00] will be used for the remaining pixel(s). Within the double word access is still low-to-high (e.g., PIX[71:64], PIX[79:72]...).

4 BPP is a special case. Within a byte, the default condition is to select first the high nibble (e.g., PIX[07:04]), then the low nibble (PIX[03:00]). The SWAP NIB bit of the Miscellaneous Control 3 register may be used to swap the order the two nibbles are used. This swap is applied to every byte that is read in, and is only active, when set, for 4 BPP.

3.3 VGA Port

VGA uses 8 bits per pixel. When the VGA port is selected only indirect mode is used. The 8 bits are masked with the Pixel Mask register and presented to the red, green, and blue palettes as indices into the 256 entries of each palette. The masked data is used as the same index into each of the three color palettes.

3.4 VRAM Pixel Port

3.4.1 4 BPP

With 4 BPP format 8 pixels (32-bit VRAM width) or 16 pixels (64-bit VRAM width) are obtained for each pixel port data access. As noted above the default access of the two pixels within each byte are high-to-low:

PIX[7:4] = pixel one

PIX[3:0] = pixel two,

but this can be reversed with the SWAP NIB bit of the Miscellaneous Control 3 register.

4 BPP is only used in indirect color mode. The 4 bits are masked with the 4 low order bits [3:0] of the Pixel Mask. The resultant masked 4 bits are then used to index into each of the red, green, and blue palettes.

With 4 BPP the 256 entry palettes are divided into 16 partitions of 16 entries per partition. The upper 4 bits of the Pixel Mask register are ignored. The PARTITION bits of the Palette Control register are used as the upper 4 bits of the palette address to select the desired partition. The 4 masked pixel bits are used to index to 1-of-16 entries within the selected partition.

As noted above 4 BPP cannot be used with a VRAM width of 128, except when "64-Bit Double Buffer Mode" is in use.

3.4.2 8 BPP

With 8 BPP format 4 pixels (32 bit VRAM width), 8 pixels (64 bit VRAM width) or 16 pixels (128 bit VRAM width) are obtained for each pixel port data access.

8 BPP can be indirect or direct, under control of the B8 DCOL bit of the 8 BPP Control register. If indirect, the 8 bits are masked with the Pixel Mask register and presented to the red, green, and blue palettes as indices into the 256 entries of each palette.

If direct, the 8 bits are presented to the red, green, and blue DACs. Note that since the red, green, and blue colors are identical the displayed image will be monochrome.

3.4.3 16 BPP

With 15 BPP or 16 BPP format 2 pixels (32-bit VRAM width), 4 pixels (64-bit VRAM width) or 8 pixels (128-bit VRAM width) are obtained for each pixel port data access. The 15 or 16 bits are expanded to 24 bits, under control of the 16 BPP Control register.

The 16 BPP Control register provides a number of options for using the 16 BPP format:

1. The incoming pixel can be 15 bits (555 format) or 16 bits (565 format).
2. The color path can be indirect (through the palettes) or direct (bypassing the palettes). Also, with 555 format, the 16th bit can be used to dynamically switch on a pixel-by-pixel basis between indirect and direct color.
3. If indirect color is selected, the addressing of the palettes can be "sparse" (pixel bits used as high order palette address bits) or "contiguous" (pixel bits used as low order palette address bits).
4. If indirect color with contiguous addressing is selected, the palettes can be divided into partitions. The PARTITION bits of the Palette Control register are used to select the partition by filling in the upper palette address bits. With 555 format 8 partitions are available; with 565 format there are 4 partitions.
5. If direct color is used the pixel bits are sent to the DAC high order bits. The low order bits can be zero filled, or the low order bits can be filled with the high order bits of the pixel data. (See description of ZIB/LIN bit below.)

If dynamic bypass is selected the following conditions will apply:

1. The format will be forced to 15 bits (555), with the unused 16th bit now used to control indirect/direct color selection.
2. The indirect color path will be forced to use sparse addressing of the palettes. Partitions cannot be used.
3. The direct color path will force the low order bits to the DACs to be zero filled (ZIB). LIN format cannot be used.
4. The Pixel Mask will mask the pixel data regardless of whether or not the palette is bypassed.

3.4.3.1 555/565 Formats

The 555/565 bit determines if the pixel is 15 bits (5:5:5 format) or 16 bits (5:6:5 format). The format designator, 5:5:5 or 5:6:5, refer to the bit allocations, high-to-low, for red:green:blue.

With 15 BPP the high order bit of each two bytes (PIX[15], PIX[31], PIX[47], PIX[63], PIX[79], PIX[95], PIX[111], PIX[127]) is discarded unless dynamic bypass is specified (B16 DCOL bits = 01). With dynamic bypass, this bit is used for indirect/direct color selection.

As noted above setting the mode to dynamic bypass will force the format to 555 regardless of the setting of the 555/565 bit.

3.4.3.2 Color Path Selection

The B16 DCOL bits are used to select one of:

1. Indirect color always (00).
2. Direct color always (11).
3. Dynamic selection of indirect or direct color (01).

The expansion to 24 bits varies depending on whether the color path is indirect or direct.

Indirect Color: The palette addressing can be sparse or contiguous and is controlled by the SPR/CNT bit. With sparse addressing the pixels will address 32 locations each for the red and blue palettes, and 32 locations for green in 555 format or 64 locations for green in 565 format. With the lower address bits set to zeroes the locations accessed will be "scattered" through the palettes, with the intermediate locations unused.

With contiguous addressing the PARTITION bits of the Palette Control register are used for the high order palette address bits, and the access within each palette is contiguous. For 555 format there are 8 partitions and 32 entries within each partition. For 565 format there are 4 partitions. All 64 entries in the green palette are addressed. Only the lower 32 entries of the red and blue palettes are used; the high 32 entries are not used.

For sparse addressing the low order bits are dependent on the ZIB/LIN bit. This bit *must* be set to 0 (ZIB). This will force the low order bits to zeros. If ZIB/LIN is 1 (LIN) then the values of the low order bits presented to the palettes are undefined.

For sparse addressing the low order Pixel Mask bits have no effect.

For contiguous addressing the high order bits are always supplied by the PARTITION bits and the high order Pixel Mask bits have no effect.

As noted above for dynamic bypass mode the format is forced to 555 mode and addressing is forced to be sparse regardless of the setting of the SPR/CNT bit.

Direct Color: To expand the 5 or 6 bits of color from the pixel data to 8 bits, the ZIB/LIN bit of the 16 BPP Control register specifies the generation of the low order 3 or 2 bits. If ZIB (Zero Intensity Black), the low order bits are made 0. If LIN (Linear), the low order bits are made equal to the high order bits. This causes the 5 or 6 bits to expand to 8 bits in a linear fashion, with both zero scale and full scale values used. With Zero Intensity Black, full scale cannot be achieved.

As noted above for dynamic bypass mode the format is forced to 555 mode and the low order fill is forced as ZIB, regardless of the setting of the ZIB/LIN bit.

3.4.3.3 Dynamic Bypass

As described above the selection of "dynamic bypass" mode forces the 555 format and uses the high order bit of the incoming 16-bit pixels as a control bit to select, on a pixel-by-pixel basis, the indirect (color lookup) or direct (lookup bypass) path.

The meaning of this bit depends on the BY16 bit in the 16 BPP Control register. When BY16 = 0 the incoming control bit forces the bypass. That is, when the control bit is 1 the palette is bypassed (direct color), and when 0 the palette is not bypassed (indirect color).

When BY16 = 1 the meaning of the incoming control bit is reversed; it now forces a lookup. That is, when the control bit is 1 the palette is used (color lookup), but when 0 the palette is bypassed (direct color).

3.4.4 24 BPP

24 BPP Packed can only be selected when the VRAM width is 64 bits or 128 bits. If 24 BPP Packed format is selected with the Pixel Format register, but the VRAM SIZE bits in the Miscellaneous Control 1 register are set for 32 bits, then the product operation is undefined.

With 24 BPP Packed format, for a VRAM width of 64 each pixel port data access contains 2+2/3 pixels. Every 3 consecutive pixel port data accesses (3 × 8 = 24 bytes) contains 8 pixels of 3 bytes each. The assignment of the bytes for each of the three accesses is shown in Figure 2 on page 15. For a VRAM width of 128 each pixel port data access contains 5+1/3 pixels. Every 3 consecutive pixel port data accesses (3 ×16 = 48 bytes) contains 16 pixels of 3 bytes each. The assignment of the bytes for each of the three accesses is shown in Figure 3 on page 15.

Each byte contains 8 bits of red, green, or blue color. Color access can be indirect or direct, and is selected with the B24P DCOL bit of the 24 BPP Packed Control register.

For indirect color, the 8 bits of red, green, and blue are each masked by the Pixel mask, and then presented to the red, green, and blue palettes as indices into the 256 entries of each palette.

For direct color, the 8 bits of red, green, and blue are presented to the DACs.

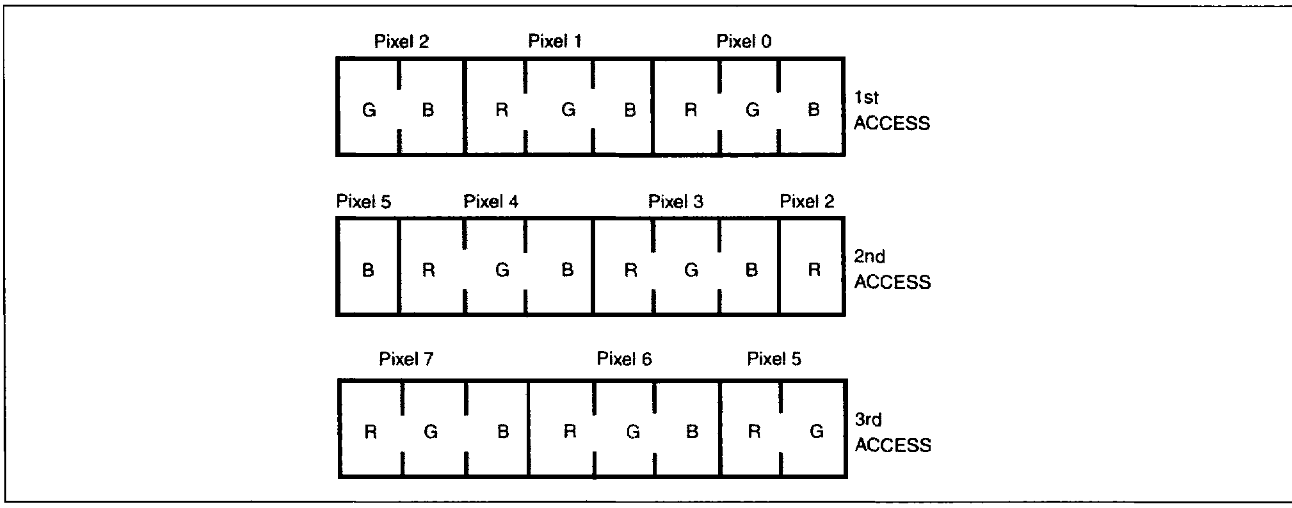


Figure 2. 24 BPP Packed Pixel Input from 64 bit VRAM

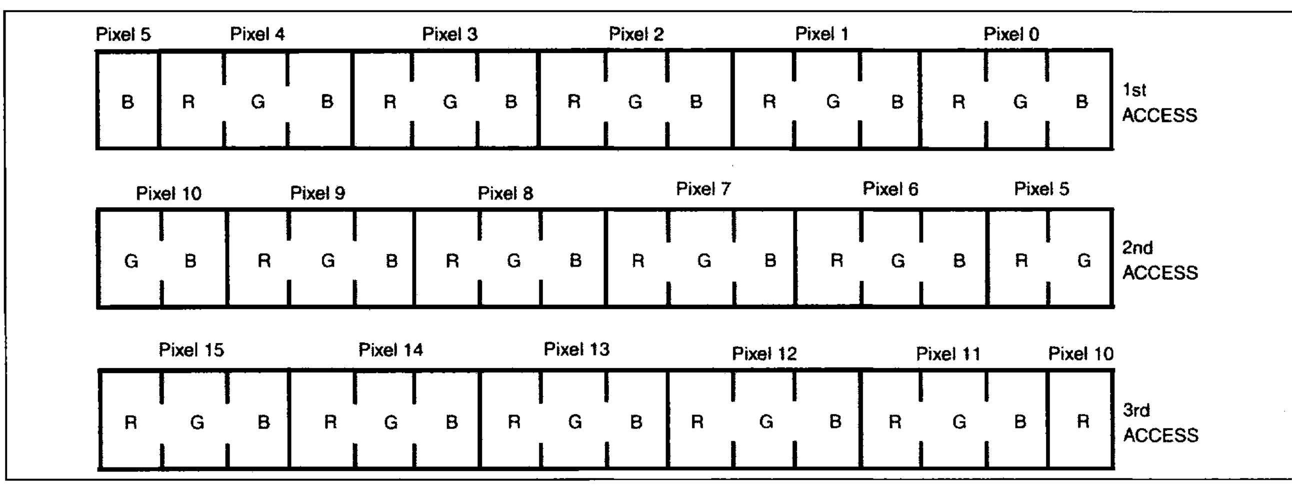


Figure 3. 24 BPP Packed Pixel Input from 128 bit VRAM

3.4.5 32 BPP

With 32 BPP format 1 pixel (32 bit VRAM width), 2 pixels (64-bit VRAM width) or 4 pixels (128-bit VRAM width) are obtained for each pixel port data access. For each 32 bits accessed, the low three bytes (24 bits) are used for the three colors, with 8 bits each for red, green, and blue.

32 BPP mode is controlled with the 32 BPP Control register. This register has the B32 DCOL bits, which are used to select one of:

1. Indirect color always (00).
2. Direct color always (11).
3. Dynamic selection of indirect or direct color (01).

With indirect color always or direct color always the high order byte is unused. (PIX[31:24], PIX[63:56], PIX[95:88] and PIX[127:120].)

With dynamic selection (dynamic bypass), the "25th" bit is used as the indirect/direct control bit (PIX[24], PIX[56], PIX[88], PIX[120]) and the remaining bits of the high order byte are unused. (PIX[31:25], PIX[63:57], PIX[95:89] and PIX[127:121].) The pixel data in this mode is masked by the Pixel Mask regardless of whether or not the palette is bypassed.

For indirect color, the 8 bits of red, green, and blue are each masked by the Pixel mask, and then presented to the red, green, and blue palettes as indices into the 256 entries of each palette.

For direct color, the 8 bits of red, green, and blue are presented to the DACs.

3.4.5.1 Dynamic Bypass

As described above the selection of "dynamic bypass" mode uses the "25th" bit of the incoming 32-bit pixels as a control bit to select, on a pixel-by-pixel basis, the indirect (color lookup) or direct (lookup bypass) path.

The meaning of this bit depends on the BY32 bit in the 32 BPP Control register. When BY32 = 0 the incoming control bit forces the bypass. That is, when the control bit is 1 the palette is bypassed (direct color), and when 0 the palette is not bypassed (indirect color).

When BY32 = 1 the meaning of the incoming control bit is reversed; it now forces a lookup. That is, when the control bit is 1 the palette is used (color lookup), but when 0 the palette is bypassed (direct color).

3.5 6 Bit Linear Palette Output

The 6BIT LIN (6 bit linear) bit of the Palette Control register affects the format of the color data read from the palettes and presented to the DACs in indirect color mode. It only has effect when the color resolution is set to 6 bits with the COL RES bit of the Miscellaneous Control 2 register and DCOL CNTL is set to indirect color.

If the palettes contain data with the two low order bits set to 00 (which will be the case when the palettes are loaded with COL RES set to 6 bits), without special processing the data values presented to the DACs will range from 0x00 through 0xfd. The maximum output of the DACs will be approximately 1.5% less than full scale (0xff). This will occur when 6BIT LIN is set to 1.

When 6BIT LIN is set to 0 (the default), then the outputs of the palettes will be modified to allow the DACs to reach full scale output. The modification consists of discarding the two low order bits from the palettes, and substituting the two high order bits for the two low order bits presented to the DACs. (i.e., the palette bits presented to a DAC will be bits 7 6 5 4 3 2 7 6).

With this bit substitution there will be a "linear" mapping of the palette data range (0x00 – 0xfd) to the DAC data range (0x00 – 0xff), and the DACs will operate over their full range.

If COL RES = 1 (8-bit color resolution) the palette outputs are presented to the DACs unchanged, and 6BIT LIN has no effect. The DACs will operate over the 8-bit range from completely off to full scale on.

Palette linear output is intended for emulation of the VGA 6-bit DACs in which the palette is loaded with 6-bit colors in the 6 high-order bits by setting COL RES to 6-bits. However, regardless of how the palette was loaded or what the pixel format is (VGA, 4, 8, 15/16, 24, 32 BPP), if enabled (DCOL = indirect, COL RES = 6 bit, 6BIT LIN = 0) the palette outputs will be affected as discussed above.

In summary, with the default conditions for VGA mode (indirect color, 6-bit color resolution, 6BIT LIN = 0), there will be a linear mapping of the 6-bit VGA palette data to the DACs, and the DACs will operate over their full range. The mapping can be turned off by setting 6BIT LIN to 1, in which case the 8 bits from the palettes are presented to the DACs unmodified. With 00 in the two low order bits of the palettes the DACs will not reach full scale output.

With 8-bit color resolution (indirect color), or with direct color, the setting of 6BIT LIN has no effect.

3.6 Double Buffer Modes

The double buffer modes are selected with the DBL BUF bits of the Miscellaneous Control 4 register. The two double buffer modes are "Dual 64-Bit Buffer" and "8 BPP Double Buffer."

3.6.1 Dual 64 Bit Buffer

This mode is only valid when the VRAM width is 128. The incoming VRAM data is considered to be from two buffers A and B, with bits[63:00] as the A buffer and bits [127:64] as the B buffer.

For a given LCLK all 128 bits are clocked in but only one set of 64 bits, A or B is used for pixel data. The other 64 bits are discarded. For the 64 bits that are used, all of VRAM pixel formats (4,8,15/16,24 packed,32 BPP, direct, indirect, etc.) are available, and are identical for each buffer. SCLK is generated as if for a VRAM width of 64 bits (see Table 2, "SCLK Frequencies," on page 5).

Although the VRAM size bits in the Miscellaneous Control 1 register must be set to a VRAM size of 128, in this double buffer mode, from a formatting and timing viewpoint, the chip operates as if the VRAM size is set to 64 bits.

If the SWAP DWRD bit is set in the Miscellaneous Control 3 register then the A and B inputs are swapped; i.e., buffer A comes from bits [127:64] and buffer B comes from bits[63:00].

3.6.2 8 BPP Double Buffer

This mode is valid for any VRAM width. The only pixel format is 8 BPP; the Pixel Format register must be set to 8 BPP or the setting of the DBL BUF bits to "8 BPP Double Buffer" in the Miscellaneous Control 4 register will be ignored. As with "regular" 8 BPP, the 8-Bit Pixel Control register can be used to select indirect or direct color.

For this mode the incoming VRAM data is grouped into 16-bit quantities, with the 16 bits representing two 8-bit pixels, A and B. Either the A or B pixel is selected for display, and the other pixel is discarded.

SCLK is generated as if the 16 BPP format was selected (see Table 2, "SCLK Frequencies," on page 5).

3.6.3 A/B Buffer Selection

For both of the dual buffer modes, the pixel selected, A or B, is determined by the BUF A/B bit of the Buffer A/B Select register. Selection is static; that is, a buffer is selected by a microprocessor write to the Buffer A/B Select register, and the chip will continuously select that buffer until the Buffer A/B Select register is changed by another microprocessor update.

There is some control of when the Buffer A/B Select register is updated. The BAB UPDT (Buffer A/B Update) bit of Miscellaneous Control 4 register determines if a write from the microprocessor bus updates the register immediately, or causes the write to be delayed internally until vertical blanking is detected. The purpose of delaying the update is to allow the buffer switch to occur between frames, during vertical blanking time.

If the delayed update is enabled it does not affect the microprocessor bus timings. The write occurs as usual, except the data is written to a temporary holding register. At vertical blanking detection whatever was last written to this holding register is what is written to the Buffer A/B Select register; if two writes occur before the update the contents of the first write will be lost.

Vertical blanking is detected by timing the $\overline{\text{BLANK}}$ signal (see 4.3, "Vertical Blanking," on page 20).

The value read back from the Buffer A/B select register, either the actual data or data that is pending from a delayed write, is controlled by the BAB RDBK bit of Miscellaneous Control 4 register.

3.7 Pixel Format Table

Table 7 shows the bit assignments of the pixel data port for each supported pixel format. Prefixes A - P identify individual pixels, and numbers 0 - 7 identify the bit within the pixel. For 4 bit pixels, this information is the data seen by the three color palettes. For 8 bit pixels, it is the data seen by the three color palettes in indirect color mode, and it is the data seen by the three DACs in direct color mode. The suffixes (blu, grn, red) identify the data seen by each of the color palettes (indirect mode) or each of the DACs (direct mode) for 16, 24, and 32 bit pixels.

Table 7. Pixel Format Table

Pixel Port Bit	4 BPP[1] SWAP NIB=0	4 BPP[1] SWAP NIB=1	8 BPP	15/16 BPP[2,3] 555 SPRSE or Direct Color	15/16 BPP 555 Contig	15/16 BPP 565 SPRSE or Direct Color	15/16 BPP 565 Contig	24 BPP Packed VRAM = 64 Bits 1st Access	24 BPP Packed VRAM = 64 Bits 2nd Access	24 BPP Packed VRAM = 64 Bits 3rd Access	24 BPP Packed VRAM = 128 Bits 1st Access	24 BPP Packed VRAM = 128 Bits 2nd Access	24 BPP Packed VRAM = 128 Bits 3rd Access	32 BPP
0	B0	A0	A0	A3BLU	A0BLU	A3BLU	A0BLU	A0BLU	C0RED	F0GRN	A0BLU	F0GRN	K0RED	A0BLU
1	B1	A1	A1	A4BLU	A1BLU	A4BLU	A1BLU	A1BLU	C1RED	F1GRN	A1BLU	F1GRN	K1RED	A1BLU
2	B2	A2	A2	A5BLU	A2BLU	A5BLU	A2BLU	A2BLU	C2RED	F2GRN	A2BLU	F2GRN	K2RED	A2BLU
3	B3	A3	A3	A6BLU	A3BLU	A6BLU	A3BLU	A3BLU	C3RED	F3GRN	A3BLU	F3GRN	K3RED	A3BLU
4	A0	B0	A4	A7BLU	A4BLU	A7BLU	A4BLU	A4BLU	C4RED	F4GRN	A4BLU	F4GRN	K4RED	A4BLU
5	A1	B1	A5	A3GRN	A0GRN	A2GRN	A0GRN	A5BLU	C5RED	F5GRN	A5BLU	F5GRN	K5RED	A5BLU
6	A2	B2	A6	A4GRN	A1GRN	A3GRN	A1GRN	A6BLU	C6RED	F6GRN	A6BLU	F6GRN	K6RED	A6BLU
7	A3	B3	A7	A5GRN	A2GRN	A4GRN	A2GRN	A7BLU	C7RED	F7GRN	A7BLU	F7GRN	K7RED	A7BLU
8	D0	C0	B0	A6GRN	A3GRN	A5GRN	A3GRN	A0GRN	D0BLU	F0RED	A0GRN	F0RED	L0BLU	A0GRN
9	D1	C1	B1	A7GRN	A4GRN	A6GRN	A4GRN	A1GRN	D1BLU	F1RED	A1GRN	F1RED	L1BLU	A1GRN
10	D2	C2	B2	A3RED	A0RED	A7GRN	A5GRN	A2GRN	D2BLU	F2RED	A2GRN	F2RED	L2BLU	A2GRN
11	D3	C3	B3	A4RED	A1RED	A3RED	A0RED	A3GRN	D3BLU	F3RED	A3GRN	F3RED	L3BLU	A3GRN
12	C0	D0	B4	A5RED	A2RED	A4RED	A1RED	A4GRN	D4BLU	F4RED	A4GRN	F4RED	L4BLU	A4GRN
13	C1	D1	B5	A6RED	A3RED	A5RED	A2RED	A5GRN	D5BLU	F5RED	A5GRN	F5RED	L5BLU	A5GRN
14	C2	D2	B6	A7RED	A4RED	A6RED	A3RED	A6GRN	D6BLU	F6RED	A6GRN	F6RED	L6BLU	A6GRN
15	C3	D3	B7	(NOTE 4)	UNUSED	A7RED	A4RED	A7GRN	D7BLU	F7RED	A7GRN	F7RED	L7BLU	A7GRN
16	F0	E0	C0	B3BLU	B0BLU	B3BLU	B0BLU	A0RED	D0GRN	G0BLU	A0RED	G0BLU	L0GRN	A0RED
17	F1	E1	C1	B4BLU	B1BLU	B4BLU	B1BLU	A1RED	D1GRN	G1BLU	A1RED	G1BLU	L1GRN	A1RED
18	F2	E2	C2	B5BLU	B2BLU	B5BLU	B2BLU	A2RED	D2GRN	G2BLU	A2RED	G2BLU	L2GRN	A2RED
19	F3	E3	C3	B6BLU	B3BLU	B6BLU	B3BLU	A3RED	D3GRN	G3BLU	A3RED	G3BLU	L3GRN	A3RED
20	E0	F0	C4	B7BLU	B4BLU	B7BLU	B4BLU	A4RED	D4GRN	G4BLU	A4RED	G4BLU	L4GRN	A4RED
21	E1	F1	C5	B3GRN	B0GRN	B2GRN	B0GRN	A5RED	D5GRN	G5BLU	A5RED	G5BLU	L5GRN	A5RED
22	E2	F2	C6	B4GRN	B1GRN	B3GRN	B1GRN	A6RED	D6GRN	G6BLU	A6RED	G6BLU	L6GRN	A6RED
23	E3	F3	C7	B5GRN	B2GRN	B4GRN	B2GRN	A7RED	D7GRN	G7BLU	A7RED	G7BLU	L7GRN	A7RED
24	H0	G0	D0	B6GRN	B3GRN	B5GRN	B3GRN	B0BLU	D0RED	G0GRN	B0BLU	G0GRN	L0RED	(NOTE 4)
25	H1	G1	D1	B7GRN	B4GRN	B6GRN	B4GRN	B1BLU	D1RED	G1GRN	B1BLU	G1GRN	L1RED	UNUSED
26	H2	G2	D2	B3RED	B0RED	B7GRN	B5GRN	B2BLU	D2RED	G2GRN	B2BLU	G2GRN	L2RED	UNUSED
27	H3	G3	D3	B4RED	B1RED	B3RED	B0RED	B3BLU	D3RED	G3GRN	B3BLU	G3GRN	L3RED	UNUSED
28	G0	H0	D4	B5RED	B2RED	B4RED	B1RED	B4BLU	D4RED	G4GRN	B4BLU	G4GRN	L4RED	UNUSED
29	G1	H1	D5	B6RED	B3RED	B5RED	B2RED	B5BLU	D5RED	G5GRN	B5BLU	G5GRN	L5RED	UNUSED
30	G2	H2	D6	B7RED	B4RED	B6RED	B3RED	B6BLU	D6RED	G6GRN	B6BLU	G6GRN	L6RED	UNUSED
31	G3	H3	D7	(NOTE 4)	UNUSED	B7RED	B4RED	B7BLU	D7RED	G7GRN	B7BLU	G7GRN	L7RED	UNUSED
32	J0	I0	E0	C3BLU	C0RED	C3BLU	C0BLU	B0GRN	E0BLU	G0RED	B0GRN	G0RED	M0BLU	B0BLU
33	J1	I1	E1	C4BLU	C1BLU	C4BLU	C1BLU	B1GRN	E1BLU	G1RED	B1GRN	G1RED	M1BLU	B1BLU
34	J2	I2	E2	C5BLU	C2BLU	C5BLU	C2BLU	B2GRN	E2BLU	G2RED	B2GRN	G2RED	M2BLU	B2BLU
35	J3	I3	E3	C6BLU	C3BLU	C6BLU	C3BLU	B3GRN	E3BLU	G3RED	B3GRN	G3RED	M3BLU	B3BLU
36	I0	J0	E4	C7BLU	C4BLU	C7BLU	C4BLU	B4GRN	E4BLU	G4RED	B4GRN	G4RED	M4BLU	B4BLU
37	I1	J1	E5	C3GRN	C0GRN	C2GRN	C0GRN	B5GRN	E5BLU	G5RED	B5GRN	G5RED	M5BLU	B5BLU
38	I2	J2	E6	C4GRN	C1GRN	C3GRN	C1GRN	B6GRN	E6BLU	G6RED	B6GRN	G6RED	M6BLU	B6BLU
39	I3	J3	E7	C5GRN	C2GRN	C4GRN	C2GRN	B7GRN	E7BLU	G7RED	B7GRN	G7RED	M7BLU	B7BLU
40	L0	K0	F0	C6GRN	C3GRN	C5GRN	C3GRN	B0RED	E0GRN	H0BLU	B0RED	H0BLU	M0GRN	B0GRN
41	L1	K1	F1	C7GRN	C4GRN	C6GRN	C4GRN	B1RED	E1GRN	H1BLU	B1RED	H1BLU	M1GRN	B1GRN
42	L2	K2	F2	C3RED	C0RED	C7GRN	C5GRN	B2RED	E2GRN	H2BLU	B2RED	H2BLU	M2GRN	B2GRN
43	L3	K3	F3	C4RED	C1RED	C3RED	C0RED	B3RED	E3GRN	H3BLU	B3RED	H3BLU	M3GRN	B3GRN
44	K0	L0	F4	C5RED	C2RED	C4RED	C1RED	B4RED	E4GRN	H4BLU	B4RED	H4BLU	M4GRN	B4GRN
45	K1	L1	F5	C6RED	C3RED	C5RED	C2RED	B5RED	E5GRN	H5BLU	B5RED	H5BLU	M5GRN	B5GRN
46	K2	L2	F6	C7RED	C4RED	C6RED	C3RED	B6RED	E6GRN	H6BLU	B6RED	H6BLU	M6GRN	B6GRN
47	K3	L3	F7	(NOTE 4)	UNUSED	C7RED	C4RED	B7RED	E7GRN	H7BLU	B7RED	H7BLU	M7GRN	B7GRN
48	N0	M0	G0	D3BLU	D0BLU	D3BLU	D0BLU	C0BLU	E0RED	H0GRN	C0BLU	H0GRN	M0RED	B0RED
49	N1	M1	G1	D4BLU	D1BLU	D4BLU	D1BLU	C1BLU	E1RED	H1GRN	C1BLU	H1GRN	M1RED	B1RED
50	N2	M2	G2	D5BLU	D2BLU	D5BLU	D2BLU	C2BLU	E2RED	H2GRN	C2BLU	H2GRN	M2RED	B2RED
51	N3	M3	G3	D6BLU	D3BLU	D6BLU	D3BLU	C3BLU	E3RED	H3GRN	C3BLU	H3GRN	M3RED	B3RED
52	M0	N0	G4	D7BLU	D4BLU	D7BLU	D4BLU	C4BLU	E4RED	H4GRN	C4BLU	H4GRN	M4RED	B4RED
53	M1	N1	G5	D3GRN	D0GRN	D2GRN	D0GRN	C5BLU	E5RED	H5GRN	C5BLU	H5GRN	M5RED	B5RED
54	M2	N2	G6	D4GRN	D1GRN	D3GRN	D1GRN	C6BLU	E6RED	H6GRN	C6BLU	H6GRN	M6RED	B6RED
55	M3	N3	G7	D5GRN	D2GRN	D4GRN	D2GRN	C7BLU	E7RED	H7GRN	C7BLU	H7GRN	M7RED	B7RED
56	P0	O0	H0	D6GRN	D3GRN	D5GRN	D3GRN	C0GRN	F0BLU	H0RED	C0GRN	H0RED	N0BLU	(NOTE 4)
57	P1	O1	H1	D7GRN	D4GRN	D6GRN	D4GRN	C1GRN	F1BLU	H1RED	C1GRN	H1RED	N1BLU	UNUSED
58	P2	O2	H2	D3RED	D0RED	D7GRN	D5GRN	C2GRN	F2BLU	H2RED	C2GRN	H2RED	N2BLU	UNUSED
59	P3	O3	H3	D4RED	D1RED	D3RED	D0RED	C3GRN	F3BLU	H3RED	C3GRN	H3RED	N3BLU	UNUSED
60	O0	P0	H4	D5RED	D2RED	D4RED	D1RED	C4GRN	F4BLU	H4RED	C4GRN	H4RED	N4BLU	UNUSED
61	O1	P1	H5	D6RED	D3RED	D5RED	D2RED	C5GRN	F5BLU	H5RED	C5GRN	H5RED	N5BLU	UNUSED
62	O2	P2	H6	D7RED	D4RED	D6RED	D3RED	C6GRN	F6BLU	H6RED	C6GRN	H6RED	N6BLU	UNUSED
63	O3	P3	H7	(NOTE 4)	UNUSED	D7RED	D4RED	C7GRN	F7BLU	H7RED	C7GRN	H7RED	N7BLU	UNUSED

Note 1: In 4 BPP mode the 4 most significant bits of each pixel come from the partition bits of the palette control register. 4 BPP is not valid with a single buffer (VRAM) width of 128.

Note 2: For 15/16 BPP Direct Color the low order bits for each color component are determined by the ZIB/LIN Bit of the 16 BPP Control register. For 15/16 BPP sparse format (indirect color), the ZIB/LIN bit must be set to ZIB, and the low order bits for each color component will be zeroes.

Note 3: In CONTIGUOUS format for 15/16 BPP the most significant bits of each pixel come from the partition bits of the palette control register.

Note 4: These bits are used for DYNAMIC BYPASS when that mode is enabled, otherwise they are unused.

Table 7. Pixel Format Table (Continued)

Pixel Port Bit	4 BPP[1] SWAP NIB=0	4 BPP[1] SWAP NIB=1	8 BPP	15/16 BPP[2,3] 555 SPRSE or Direct Color	15/16 BPP 555 Contig	15/16 BPP 565 SPRSE or Direct Color	15/16 BPP 565 Contig	24 BPP Packed VRAM = 64 Bits 1st Access	24 BPP Packed VRAM = 64 Bits 2nd Access	24 BPP Packed VRAM = 64 Bits 3rd Access	24 BPP Packed VRAM = 128 Bits 1st Access	24 BPP Packed VRAM = 128 Bits 2nd Access	24 BPP Packed VRAM = 128 Bits 3rd Access	32 BPP
64			I0	E3BLU	E0BLU	E3BLU	E0BLU				C0RED	I0BLU	N0GRN	C0BLU
65			I1	E4BLU	E1BLU	E4BLU	E1BLU				C1RED	I1BLU	N1GRN	C1BLU
66			I2	E5BLU	E2BLU	E5BLU	E2BLU				C2RED	I2BLU	N2GRN	C2BLU
67			I3	E6BLU	E3BLU	E6BLU	E3BLU				C3RED	I3BLU	N3GRN	C3BLU
68			I4	E7BLU	E4BLU	E7BLU	E4BLU				C4RED	I4BLU	N4GRN	C4BLU
69			I5	E3GRN	E0GRN	E2GRN	E0GRN				C5RED	I5BLU	N5GRN	C5BLU
70			I6	E4GRN	E1GRN	E3GRN	E1GRN				C6RED	I6BLU	N6GRN	C6BLU
71			I7	E5GRN	E2GRN	E4GRN	E2GRN				C7RED	I7BLU	N7GRN	C7BLU
72			J0	E6GRN	E3GRN	E5GRN	E3GRN				D0BLU	I0GRN	N0RED	C0GRN
73			J1	E7GRN	E4GRN	E6GRN	E4GRN				D1BLU	I1GRN	N1RED	C1GRN
74			J2	E3RED	E0RED	E7GRN	E5GRN				D2BLU	I2GRN	N2RED	C2GRN
75			J3	E4RED	E1RED	E3RED	E0RED				D3BLU	I3GRN	N3RED	C3GRN
76			J4	E5RED	E2RED	E4RED	E1RED				D4BLU	I4GRN	N4RED	C4GRN
77			J5	E6RED	E3RED	E5RED	E2RED				D5BLU	I5GRN	N5RED	C5GRN
78			J6	E7RED	E4RED	E6RED	E3RED				D6BLU	I6GRN	N6RED	C6GRN
79			J7	(NOTE 4)	UNUSED	E7RED	E4RED				D7BLU	I7GRN	N7RED	C7GRN
80			K0	F3BLU	F0BLU	F3BLU	F0BLU				D0GRN	I0RED	O0BLU	C0RED
81			K1	F4BLU	F1BLU	F4BLU	F1BLU				D1GRN	I1RED	O1BLU	C1RED
82			K2	F5BLU	F2BLU	F5BLU	F2BLU				D2GRN	I2RED	O2BLU	C2RED
83			K3	F6BLU	F3BLU	F6BLU	F3BLU				D3GRN	I3RED	O3BLU	C3RED
84			K4	F7BLU	F4BLU	F7BLU	F4BLU				D4GRN	I4RED	O4BLU	C4RED
85			K5	F3GRN	F0GRN	F2GRN	F0GRN				D5GRN	I5RED	O5BLU	C5RED
86			K6	F4GRN	F1GRN	F3GRN	F1GRN				D6GRN	I6RED	O6BLU	C6RED
87			K7	F5GRN	F2GRN	F4GRN	F2GRN				D7GRN	I7RED	O7BLU	C7RED
88			L0	F6GRN	F3GRN	F5GRN	F3GRN				D0RED	J0BLU	O0GRN	(NOTE 4)
89			L1	F7GRN	F4GRN	F6GRN	F4GRN				D1RED	J1BLU	O1GRN	UNUSED
90			L2	F3RED	F0RED	F7GRN	F5GRN				D2RED	J2BLU	O2GRN	UNUSED
91			L3	F4RED	F1RED	F3RED	F0RED				D3RED	J3BLU	O3GRN	UNUSED
92			L4	F5RED	F2RED	F4RED	F1RED				D4RED	J4BLU	O4GRN	UNUSED
93			L5	F6RED	F3RED	F5RED	F2RED				D5RED	J5BLU	O5GRN	UNUSED
94			L6	F7RED	F4RED	F6RED	F3RED				D6RED	J6BLU	O6GRN	UNUSED
95			L7	(NOTE 4)	UNUSED	F7RED	F4RED				D7RED	J7BLU	O7GRN	UNUSED
96			M0	G3BLU	G0RED	G3BLU	G0BLU				E0BLU	J0GRN	O0RED	D0BLU
97			M1	G4BLU	G1BLU	G4BLU	G1BLU				E1BLU	J1GRN	O1RED	D1BLU
98			M2	G5BLU	G2BLU	G5BLU	G2BLU				E2BLU	J2GRN	O2RED	D2BLU
99			M3	G6BLU	G3BLU	G6BLU	G3BLU				E3BLU	J3GRN	O3RED	D3BLU
100			M4	G7BLU	G4BLU	G7BLU	G4BLU				E4BLU	J4GRN	O4RED	D4BLU
101			M5	G3GRN	G0GRN	G2GRN	G0GRN				E5BLU	J5GRN	O5RED	D5BLU
102			M6	G4GRN	G1GRN	G3GRN	G1GRN				E6BLU	J6GRN	O6RED	D6BLU
103			M7	G5GRN	G2GRN	G4GRN	G2GRN				E7BLU	J7GRN	O7RED	D7BLU
104			N0	G6GRN	G3GRN	G5GRN	G3GRN				E0GRN	J0RED	P0BLU	D0GRN
105			N1	G7GRN	G4GRN	G6GRN	G4GRN				E1GRN	J1RED	P1BLU	D1GRN
106			N2	G3RED	G0RED	G7GRN	G5GRN				E2GRN	J2RED	P2BLU	D2GRN
107			N3	G4RED	G1RED	G3RED	G0RED				E3GRN	J3RED	P3BLU	D3GRN
108			N4	G5RED	G2RED	G4RED	G1RED				E4GRN	J4RED	P4BLU	D4GRN
109			N5	G6RED	G3RED	G5RED	G2RED				E5GRN	J5RED	P5BLU	D5GRN
110			N6	G7RED	G4RED	G6RED	G3RED				E6GRN	J6RED	P6BLU	D6GRN
111			N7	(NOTE 4)	UNUSED	G7RED	G4RED				E7GRN	J7RED	P7BLU	D7GRN
112			O0	H3BLU	H0BLU	H3BLU	H0BLU				E0RED	K0BLU	P0GRN	D0RED
113			O1	H4BLU	H1BLU	H4BLU	H1BLU				E1RED	K1BLU	P1GRN	D1RED
114			O2	H5BLU	H2BLU	H5BLU	H2BLU				E2RED	K2BLU	P2GRN	D2RED
115			O3	H6BLU	H3BLU	H6BLU	H3BLU				E3RED	K3BLU	P3GRN	D3RED
116			O4	H7BLU	H4BLU	H7BLU	H4BLU				E4RED	K4BLU	P4GRN	D4RED
117			O5	H3GRN	H0GRN	H2GRN	H0GRN				E5RED	K5BLU	P5GRN	D5RED
118			O6	H4GRN	H1GRN	H3GRN	H1GRN				E6RED	K6BLU	P6GRN	D6RED
119			O7	H5GRN	H2GRN	H4GRN	H2GRN				E7RED	K7BLU	P7GRN	D7RED
120			P0	H6GRN	H3GRN	H5GRN	H3GRN				F0BLU	K0GRN	P0RED	(NOTE 4)
121			P1	H7GRN	H4GRN	H6GRN	H4GRN				F1BLU	K1GRN	P1RED	UNUSED
122			P2	H3RED	H0RED	H7GRN	H5GRN				F2BLU	K2GRN	P2RED	UNUSED
123			P3	H4RED	H1RED	H3RED	H0RED				F3BLU	K3GRN	P3RED	UNUSED
124			P4	H5RED	H2RED	H4RED	H1RED				F4BLU	K4GRN	P4RED	UNUSED
125			P5	H6RED	H3RED	H5RED	H2RED				F5BLU	K5GRN	P5RED	UNUSED
126			P6	H7RED	H4RED	H6RED	H3RED				F6BLU	K6GRN	P6RED	UNUSED
127			P7	(NOTE 4)	UNUSED	H7RED	H4RED				F7BLU	K7GRN	P7RED	UNUSED

Note 1: In 4 BPP mode the 4 most significant bits of each pixel come from the partition bits of the palette control register. 4 BPP is not valid with a single buffer (VRAM) width of 128.

Note 2: For 15/16 BPP Direct Color the low order bits for each color component are determined by the ZIB/LIN Bit of the 16 BPP Control register. For 15/16 BPP sparse format (indirect color), the ZIB/LIN bit must be set to ZIB, and the low order bits for each color component will be zeroes.

Note 3: In CONTIGUOUS format for 15/16 BPP the most significant bits of each pixel come from the partition bits of the palette control register.

Note 4: These bits are used for DYNAMIC BYPASS when that mode is enabled, otherwise they are unused.

4.0 Controls

4.1 Blank and Border Control

The BLANK and BORDER/OE signals control the way in which data is presented to the DACs. These control signals are used to determine when pixel data is valid, when the border color is to be displayed, where the cursor should be located on the screen, and how the MISR will accumulate its signature.

4.2 Blanking Control

BLANK is latched by the rising edge of LCLK. When BLANK is active (low), the data presented to the DACs is forced to zeroes. When BLANK is inactive (high), the pixel data or VGA data is considered valid (unless BORDER is active), and the data is presented to the DACs as determined by the current mode of operation. Cursor data will override pixel data when the cursor is to be displayed.

4.3 Vertical Blanking

When BLANK is active (low) an internal counter is used to determine whether or not the current blanking interval is vertical blanking. If the counter reaches its maximum count of 2048 pixels, an internal signal will become active to indicate that the end of the current frame has been reached. This internal signal will remain active until BLANK becomes inactive (high). This vertical blanking detection is used by the cursor logic to position the cursor (if enabled) in the following frame. It is also used by the MISR (if enabled) to control the accumulation of a signature for one complete frame of pixel data. Also, if enabled, vertical blanking detection is used to control the loading of the Buffer A/B Select register for use with double buffer modes.

4.4 Border Control

BORDER/OE is a shared function input. It can indicate either "Border" time, for displaying a border, or "Odd/Even" for use with interlace mode. The usage of this pin is determined by the BRDR/INTL of the Miscellaneous Control 2 register. When used as a border control interlace mode is not supported with display of the hardware cursor.

When used as BORDER, the input is latched by the rising edge of LCLK. When BLANK is active (low), BORDER must also be active (low). When BLANK is inactive (high), the state of BORDER will determine whether or not the color in the Border Color registers is displayed. If BORDER is active (low), the border color is displayed, and if BORDER is inactive (high), the pixel data or cursor data is displayed. For cursor positioning, the active display area is considered valid when BORDER and BLANK are both inactive (high). The MISR signature is accumulated when BLANK alone is inactive (high), thus the border area is included in the MISR accumulation. If no border is required, the BORDER input should be tied to BLANK.

The intent of the BORDER signal is to create a "picture frame" around the active display area. BORDER can remain active (low) for entire scan lines at the top and bottom of the active display area, or it can be active at the beginning and end of each scan line to create this effect. Other changes in the BORDER signal within the active display area are not allowed.

If the BRDR/INTL bit in Miscellaneous Control 2 is set to "INTL" operation, no border will be displayed.

4.5 Sync Control

Three sync signals are brought into the device on two pins, HCSYNCIN and VSYNCIN.

Four registers control what is done with these signals:

- Sync Control (index 0x0003)
- Horizontal Sync Position (index 0x0004)
- DAC Operation (index 0x0006)
- Power Management (index 0x0005)

Horizontal sync on HCSYNCIN is processed and sent out on HSYNCOUT. Vertical sync on VSYNCIN is processed and sent out on VSYNCOUT.

The intent of processing horizontal sync is to delay it to match the delay seen by the pixel data from the inputs (VGA[7:0] or PIX[127:0]) to the DAC outputs. In addition, the signal may be inverted, forced low or high, or 3-stated.

A mismatch between pixel delay and horizontal sync delay can cause a visible effect, that is, the display may not be centered horizontally on the screen. The vertical display timings are generally such that mismatches are not visible. Vertical sync is brought in on VSYNCIN and sent out on VSYNCOUT to provide the same invert, force low or high, and 3-state controls as provided for horizontal sync.

Composite sync on HCSYNCIN may be injected onto the Green DAC output for composite-sync-on-green. This function is enabled by setting the SOG bit of the DAC Operation register. If this bit is off HCSYNCIN is not used for composite sync.

The composite sync is delayed internally to match the pixel pipeline delay.

Since horizontal and composite sync are shared, only one of them should be enabled at a given time. For example, if the signal on HCSYNCIN is horizontal sync, then the SOG bit on the DAC control register should be off. Or, if SOG is on to inject composite sync on HCSYNCIN onto the green DAC output, some decision must be made on how to handle the HSYNCOUT output (force low, high, 3-state, or leave unconnected).

4.6 Clocking and Pipeline Delay

4.6.1 Horizontal Sync

The clocking and delay of HCSYNCIN to HSYNCOUT depends on the DLY CNTL bit of the Sync Control register. If this bit is set to 1, HCSYNCIN is passed directly to HSYNCOUT without latching and without pipeline delay matching.

If DLY CNTL is set to 0 and SOG is off (no composite sync), then HCSYNCIN is latched on the rising edge of LCLK and delayed internally to match the pixel pipeline delay before being sent out on HSYNCOUT. Also, additional delay may be added with the Horizontal Position register (see section below).

If SOG is on (composite sync) then DLY CNTL has no effect and HCSYNCIN is passed directly to HSYNCOUT without latching and without pipeline delay matching. (This is not a typical use for this input, it is just a byproduct of sharing horizontal sync with composite sync.)

4.6.2 Vertical Sync

VSYNCIN is passed directly to VSYNCOUT without latching and without pipeline delay matching.

4.6.3 Composite Sync

The HCSYNCIN input is always latched on the rising edge of LCLK for use as composite sync. When enabled with the SOG bit, it is delayed internally to match the pipeline delay of the pixel data, and then is injected onto the Green DAC output. As with horizontal sync, additional delay can be added with the Horizontal Sync Position register.

4.6.4 Horizontal Position Control

Additional delay of 0 to 15 pixel clock periods may be added to the horizontal sync and composite sync signals with the Horizontal Sync Position register.

The intent of this additional delay is to provide a "fine tune" control of the horizontal screen position. Typically the incoming sync signals can only be adjusted in multiples of the pixel clock. The additional delay added with the Horizontal Position Control register adjusts the screen position with pixel increments.

The Horizontal Position register can be used on horizontal sync when DLY CNTL is set to 0 and SOG is off. The register can be used with composite sync when SOG is on.

4.7 Additional Sync Control

The polarity of the received HCSYNCIN input may be inverted before it is applied to the green DAC using the CSYN INVT bit of the Sync Control register.

The polarity may be inverted between HCSYNCIN and HSYNCOUT using the HSYN INVT bit, and the polarity may be inverted between VSYNCIN and VSYNCOUT using the VSYN INVT bit.

The HSYNCOUT and VSYNCOUT signals may be individually forced low, forced high, or forced to high impedance using the HSYN CNTL and VSYN CNTL bits of the Sync Control register.

As discussed in 8.3, "Clocking Power," on page 29, the clocks to the sync delay circuits can be shut off with the SYNC PWR bit of the Power Management register.

4.8 24 Bit Packed Pixel Control

The 24 bit packed pixel format requires special consideration.

For a VRAM width of 64 the pixel data at the beginning of a line must be aligned on an 8-pixel boundary as shown in Figure 2 on page 15. These 8 pixels correspond to three 64-bit pixel port loads or three SCLK cycles.

For a VRAM width of 128 the pixel data at the beginning of a line must be aligned on a 16 pixel boundary as shown in Figure 3 on page 15. These 16 pixels correspond to three 128-bit pixel port loads, which is also three SCLK cycles.

In order to keep pixel data and control signals properly aligned, all control signals ($\overline{\text{BLANK}}$, $\overline{\text{BORDER/OE}}$, $\overline{\text{HCSYNCIN}}$ and $\overline{\text{VSYNCIN}}$) are required to change in increments of 8 pixels (VRAM width = 64) or 16 pixels (VRAM width = 128). There are 3 SCLKS per increment in either case.

When either $\overline{\text{BLANK}}$ or $\overline{\text{BORDER/OE}}$ changes to indicate the beginning of an active display line, it is assumed that the pixel data which begins that line is aligned on the proper 8 (16) pixel boundary.

5.0 Cursor Operation

The cursor is a 32x32 or 64x64 pixel pattern that is overlaid on the display pixels just before presentation to the DACs. The cursor size, 32x32 or 64x64 is set with the CURS SIZE bit of the Cursor Control register.

Pixel columns are numbered left to right starting with 0. Pixel rows are numbered top to bottom starting with 0.

5.1 Cursor Enable

The cursor is enabled when the CURSOR MODE bits of the Cursor Control register are not 00. When enabled, the cursor will display if it has not been moved off-screen. If disabled (CURSOR MODE = 00), the cursor will not be displayed.

The cursor may be used with either pixel port (VGA or PIX), with any of the pixel formats (VGA, 4, 8, 15/16, 24, 32 BPP), and with indirect or direct color.

5.2 Cursor Array

The cursor image is stored in the Cursor Array. The array is organized 1024x8 (1024 bytes). It is accessed as Indexed Data using index addresses 0x0100 through 0x04ff.

Each pixel of the cursor uses 2 bits, thus 4 cursor pixels are stored in each byte of the array. The entire array is used to contain the 64x64 cursor image (4 pixels/byte × 1024 bytes = 4096 pixels = 64x64).

For the 32x32 cursor only 256 bytes are required (4 pixels/byte × 256 bytes = 1024 pixels = 32x32.) The cursor array is divided into 4 contiguous slots to allow the storage of 4 cursor images. The SMLC SLOT bits of the Cursor Control register are used to select one of the four slots for display. The SMLC SLOT bits have no effect when the cursor size is 64x64.

Storage of the cursor within the array starts with the top row. For the 64x64 cursor the first 16 bytes hold row 0, the next 16 bytes hold row 1, and so on, starting with the first byte in the array at index address 0x0100.

For the 32x32 cursor the first 8 bytes hold row 0, the next 8 bytes hold row 1, and so on, starting with the first byte in a slot (index addresses 0x0100, 0x0200, 0x0300 or 0x0400).

Within a row the pixels are stored left to right in groups of four. The first byte holds pixels 0, 1, 2, 3, the next byte holds pixels 4, 5, 6, 7, and so on.

Within a byte the four pixels may be stored right to left or left to right, depending on the PIX ORDR bit of the Cursor Control register. If PIX ORDR = 0 the pixels are stored right to left (3, 2, 1, 0); if PIX ORDR = 1 the pixels are stored left to right (0, 1, 2, 3).

5.2.1 Cursor Array Access

Cursor Array writes and reads are synchronized with the internal pixel clock, so the pixel clock must be running for microprocessor accesses to be valid. If this condition is met, the cursor array may be written or read at any time.

Microprocessor read accesses of the cursor array may disturb the cursor image if it is being displayed at that time. However, no more than one cursor pixel will be disturbed per cursor read access. Microprocessor write accesses of the cursor array will not disturb the cursor.

5.2.2 Cursor Array Writes

A write to the cursor array is accomplished by writing the Index High and Index Low registers with an index address for the array (0x0100 – 0x04ff), followed by a write of the desired data to Index Data. If auto-increment is turned on, the entire array may be written sequentially by repeated writes to Index Data.

5.2.3 Cursor Array Reads

To meet the bus timings for reads, the cursor array read data is pre-fetched. A pre-fetch is triggered by writing the Index High or Index Low register such that the resulting index address is for an entry in the array (0x0100 -- 0x04ff). At the end of the write cycle the cursor array will be read at the address held in the index address registers, and the read data will be held in an internal register. A subsequent read of Index Data will read this pre-fetched data. At the end of the read another pre-fetch will be triggered. If auto-increment is turned on, this pre-fetch will be for the next address in the array. Thus, the entire array can be read by repeated reads from Index Data.

The pre-fetching of cursor array data will stop if

1. The index register auto-increments beyond 0x04ff

   OR

2. A write is done to Index Data.

5.3 Cursor Modes

Each pixel of the cursor is specified with 2 bits. There are three ways that these 2 bits can be used, as specified by the CURSOR MODE bits of the Cursor Control register. These are shown in Table 8, "Cursor Modes," on page 25.

There are three cursor colors that may be displayed. The colors are stored in the Cursor Color 1 Red, Green, Blue, Cursor Color 2 Red, Green, Blue, and Cursor Color 3 Red, Green, Blue registers. Each red, green, and blue register is 8 bits, yielding a full 24-bit color for each of the three cursor colors. The cursor color is always 24 bits, and is not affected by the COL RES or 6BIT LIN control bits, or any of the pixel formats (VGA, 4, 8, 15/16, 24, 32 BPP).

Cursor Mode 0 allows selection of any of the three colors while Modes 1 and 2 allow selection between colors 1 and 2.

All modes can specify that the cursor pixel be transparent, to allow the underlying display pixel to be displayed. This pixel will either be a palette output or a formatted VRAM pixel, depending on whether the pixel format is VGA or indirect color, or direct color.

Mode 1 can also specify that the complement of the underlying display pixel be displayed. The intent is to highlight the cursor by "reversing" the color of the background pixels.

5.4 Cursor Hot Spot

The hot spot is the point within the cursor that is used to locate the cursor's position on the screen. Any pixel within the cursor may be identified as the hot spot.

The Cursor Hot Spot X and Cursor Hot Spot Y registers hold the unsigned cursor pixel X (column) and Y (row) coordinates for the hot spot. The range for the X and Y values is 0 to 31 for the 32x32 cursor and 0 to 63 for the 64x64 cursor.

5.5 Cursor Position

The Cursor X Low, Cursor X High, Cursor Y Low, and Cursor Y High registers specify the position of the cursor (the cursor hot spot) on the screen.

The X and Y positions are specified as *signed* numbers in two's complement format. The High and Low pairs yield 16-bit position registers, of which 12 bits plus a sign bit are used.

The hardware automatically extends the sign bit into the unused bit positions of the position registers. The valid X and Y ranges are -4096 to +4095.

The X and Y screen coordinates are for non-border display pixels. (0,0) is the upper left corner pixel of the screen that is not in the border area. The X value increases positively left-to-right, and the Y value increases positively top-to-bottom. Negative X values are to the left of the non-border display area and negative Y values are above the top of the non-border display area.

The cursor is clipped by the edges of the screen if there is no border, or by the border if a border is used. For example, if the hot spot is (0,0) the full cursor will be displayed in the upper left corner if the X position is +0 and the Y position is +0. If the X value is changed to -1 (0xffff) only columns 1 through 31 of the cursor will be displayed. If the X value is -31 (0xffe1) only column 31 of the cursor will be displayed. If the X value is more negative than -31 the cursor will not be displayed.

5.6 Interlace

The selection of cursor rows for display is changed if interlace mode is specified. This is controlled with the INTL MODE bit of the Miscellaneous Control 2 register.

In non-interlaced mode, the cursor rows are displayed sequentially, starting with the first non-clipped row to be displayed based on the Y position and Y Hot Spot register contents.

When interlaced mode is specified, the ODD/$\overline{\text{EVEN}}$ signal (actually $\overline{\text{BORDER}}$/$\overline{\text{OE}}$, see below) is used to determine if odd or even scan lines are being displayed. If ODD/$\overline{\text{EVEN}}$ is low (even field), the first non-clipped cursor row that falls on an even scan line is displayed. Similarly, if ODD/$\overline{\text{EVEN}}$ is high (odd field), the first non-clipped cursor row that falls on an odd scan line is displayed. In either case, if the first cursor line displayed is an even-numbered cursor row (as determined by Y Position and Y Hot Spot) then successive even-numbered cursor rows will be displayed during that field. If the first cursor line displayed is an odd-numbered cursor row then successive odd-numbered cursor rows will be displayed during that field.

ODD/$\overline{\text{EVEN}}$ should only change during vertical blanking time for proper cursor display.

The ODD/$\overline{\text{EVEN}}$ input is actually the shared input pin $\overline{\text{BORDER}}$/$\overline{\text{OE}}$, where the usage of the pin is determined by the BRDR/INTL of the Miscellaneous Control 2 register. BRDR/INTL must be set to INTL for using the cursor with interlaced mode. If BRDR/INT is set as BRDR then the INTL MODE bit will be ignored (non-interlaced mode will be used).

5.7 Cursor Update and Display

5.7.1 Position

Writing any of the Cursor X Low, Cursor X High, or Cursor Y Low registers will not affect the position of the cursor on the screen. When the Cursor Y High register is written, the X and Y positions are captured in a second set of registers.

When vertical blanking is detected (see 4.3, "Vertical Blanking," on page 20), the "captured" X and Y positions are sampled. The sampled position is saved until it is resampled on the next vertical blanking time. Between vertical blanking times the sampled position is used, along with the Cursor Hot Spot, to calculate which pixels of the cursor are used and where they are displayed on the screen.

When INTL MODE is set the ODD/$\overline{\text{EVEN}}$ signal is examined at the end of vertical blanking to determine if only even or only odd rows will be displayed.

5.7.2 Controls

When vertical blanking is detected the Cursor Control register is sampled along with the X and Y position registers. This allows the cursor to be toggled on and off on a frame-by-frame basis with the CURSOR MODE bits, and if the cursor is 32x32, it allows toggling among the four slots on a frame-by-frame basis using the SMLC SLOT bits.

Note that in interlace mode the sampling is on a field-by-field basis. Also, since the PIX ORDER and CURS SIZE bits are also sampled these functions will only change when vertical blanking is detected.

5.7.3 Other

Changes to the Cursor Color registers and the Cursor X and Y Hot Spot registers are propagated to the cursor logic as soon as they are made, so if they are updated while the cursor is being displayed the cursor image will be disturbed.

Changes to the cursor array are also propagated to the cursor logic as soon as they are made. Also, as noted above, microprocessor read accesses of the cursor array may interfere with the cursor display logic. For example, with a 32x32 cursor being displayed from slot 0, microprocessor read accesses to slot 1 may cause the display of the slot 0 cursor to be disturbed.

It is recommended that Cursor Array Reads and changes to the Cursor Color registers and the Cursor X and Y Hot Spot registers be made only when the cursor is disabled, off screen, or during vertical blanking time.

Table 8. Cursor Modes

CURSOR PIXELS	CURSOR MODE		
	Mode 0 CURSOR MODE = 01	Mode 1 CURSOR MODE = 10	Mode 2 CURSOR MODE = 11
00	Transparent	Cursor Color 1	Transparent
01	Cursor Color 1	Cursor Color 2	Transparent
10	Cursor Color 2	Transparent	Cursor Color 1
11	Cursor Color 3	Complement	Cursor Color 2

6.0 DAC Control

Several miscellaneous features of the DACs are controlled by the DAC Operation register.

6.1 SOG - Composite Sync-On-Green

When the SOG bit is set, the signal on the $\overline{\text{HCSYNCIN}}$ input will be merged with the pixel data on the green DAC. The incoming signal may be inverted and/or delayed before presentation at the DAC.

6.2 BRB - Blank Red and Blue DACs

When this is set the red and blue DACs are set to the blanking level. This is intended for use when a monochrome display is driven by the green DAC.

6.3 DSR - DAC Slew Rate

This bit can be written and read but has no effect. On the original RGB528A this bit controlled the Slew Rate of the DACs (slow or fast). On the "-A" revision this bit is disconnected; the DACs are always set to the "fast" slew rate setting.

6.4 DPE - DAC Blanking Pedestal Enable

When off, the DAC pedestal is disabled (blanking level = 0 IRE). When on, the pedestal is enabled (7.5 IRE).

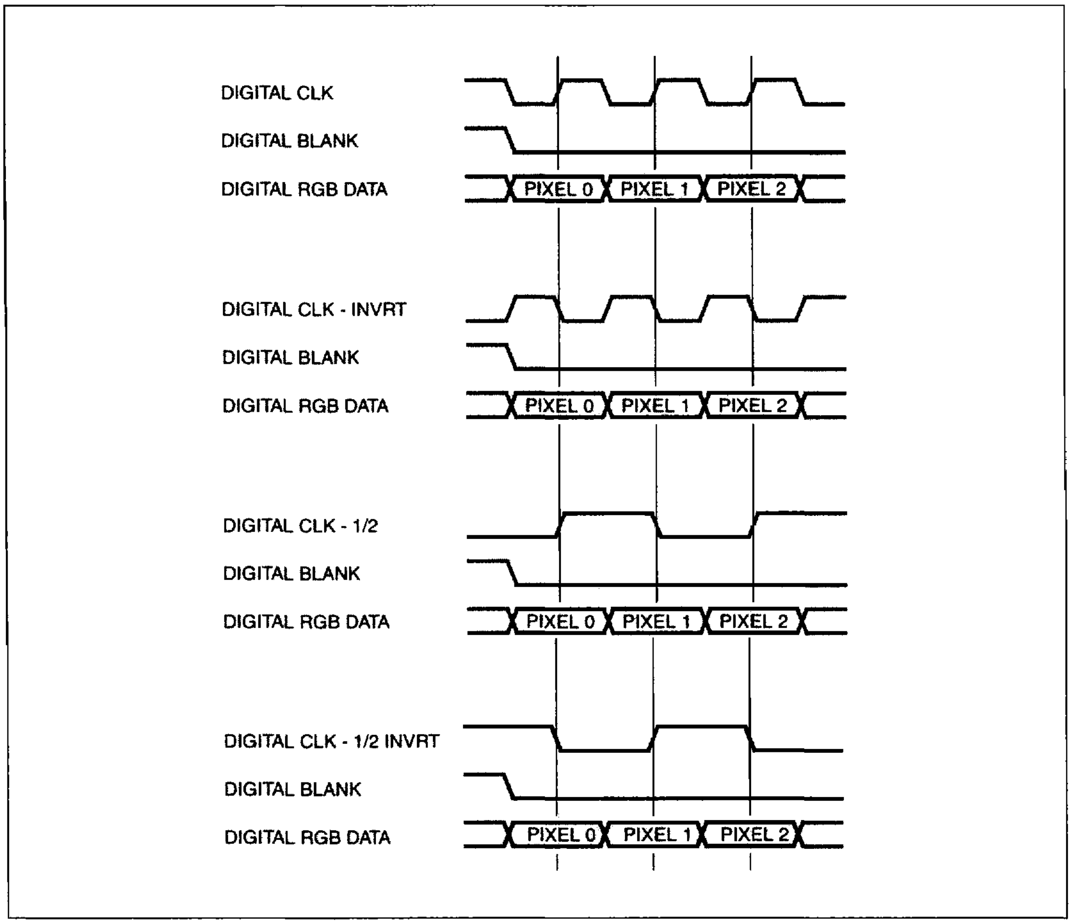


Figure 4. Digital Output Clocking Options

7.0 Digital Outputs

The digital pixel data that is presented internally to the DACs is made available externally for driving flat panel displays. There are two restrictions:

- The VRAM size cannot be 128, because the digital outputs are shared with the high 64 VRAM pixel inputs.
- The digital clock output cannot be faster than 55 MHz.

The digital outputs are enabled by setting the DIGI MODE bits of the Miscellaneous Control 4 register. However, if the VRAM size is set to 128 these bits are ignored, and the digital outputs are disabled (3-stated).

7.1 Output Signals

The following signals are provided for the digital interface:

1. DIGI CLK - the internal pixel clock.
2. DIGI BLANK - This output is high during blanking and low during active picture time. It is the same as the $\overline{\text{BLANK}}$ input signal, except inverted, synchronized with the DIGI CLK output, and delayed internally to match the same pipeline delay as the pixels.
3. DIGI DATA - the pixel data, eight bits each for red, green, and blue.

7.2 Clocking Options

The default configuration has the pixel data valid when the clock goes from low to high, for external latching of the pixel data using the up-going edge. Miscellaneous Control 4 register has two bits for changing this operation.

DIGI CINV - Digital Clock Invert. When this bit is set the clock is inverted. This allows the pixels to be latched on the down-going edge.

DIGI CDIV - Digital Clock Divide. When this bit is set the outgoing DIGI CLK is the pixel clock divided by 2. The intent of this is to have the even pixels latched on the up-going edge and the odd pixels latched on the down-going edge.

Both bits can be set, such that the clock is both divided in half and inverted. This is the condition for having the even pixels latched on the down-going edge and the odd pixels latched on the up-going edge.

All four combinations of clock options are shown in Figure 4 on page 26.

7.3 Pixel Formats

The pixel data on the digital outputs have three formats, selected with the DIGI MODE bits of the Miscellaneous Control 4 register.

1. 4 Bit Output - the four high order bits of each color, red, green, and blue, are presented on the four high order bits of each 8-bit digital output group. The four low order bits of each color are set to high impedance and never change.
2. 4 Bit Output Replicated - This is the same as above, with the four high order pixel bits driven on the four high order digital outputs for each color, but in addition, for each color, the high order pixel bits are also presented on the four low order digital outputs.
3. 8 Bit Output - For each color, all 8 internal pixel bits are brought out on the digital outputs.

A mapping of the bits for each format to the digital output bit positions is given in Table 9 on page 28.

Table 9. Digital Output Formats

VRAM Inputs	Digital Outputs	Digital Output Formats		
		4 Bit Output with High-Z (DIGIMODE = 01)	4 Bit Output Replicated (DIGIMODE = 10)	8 Bit Output (DIGIMODE = 11)
PIX[64]	DIGITAL BLUE[0]	High-Z	BLUE[4]	BLUE[0]
PIX[65]	DIGITAL BLUE[1]	High-Z	BLUE[5]	BLUE[1]
PIX[66]	DIGITAL BLUE[2]	High-Z	BLUE[6]	BLUE[2]
PIX[67]	DIGITAL BLUE[3]	High-Z	BLUE[7]	BLUE[3]
PIX[68]	DIGITAL BLUE[4]	BLUE[4]	BLUE[4]	BLUE[4]
PIX[69]	DIGITAL BLUE[5]	BLUE[5]	BLUE[5]	BLUE[5]
PIX[70]	DIGITAL BLUE[6]	BLUE[6]	BLUE[6]	BLUE[6]
PIX[71]	DIGITAL BLUE[7]	BLUE[7]	BLUE[7]	BLUE[7]
PIX[72]	DIGITAL GREEN[0]	High-Z	GREEN[4]	GREEN[0]
PIX[73]	DIGITAL GREEN[1]	High-Z	GREEN[5]	GREEN[1]
PIX[74]	DIGITAL GREEN[2]	High-Z	GREEN[6]	GREEN[2]
PIX[75]	DIGITAL GREEN[3]	High-Z	GREEN[7]	GREEN[3]
PIX[76]	DIGITAL GREEN[4]	GREEN[4]	GREEN[4]	GREEN[4]
PIX[77]	DIGITAL GREEN[5]	GREEN[5]	GREEN[5]	GREEN[5]
PIX[78]	DIGITAL GREEN[6]	GREEN[6]	GREEN[6]	GREEN[6]
PIX[79]	DIGITAL GREEN[7]	GREEN[7]	GREEN[7]	GREEN[7]
PIX[80]	DIGITAL RED[0]	High-Z	RED[4]	RED[0]
PIX[81]	DIGITAL RED[1]	High-Z	RED[5]	RED[1]
PIX[82]	DIGITAL RED[2]	High-Z	RED[6]	RED[2]
PIX[83]	DIGITAL RED[3]	High-Z	RED[7]	RED[3]
PIX[84]	DIGITAL RED[4]	RED[4]	RED[4]	RED[4]
PIX[85]	DIGITAL RED[5]	RED[5]	RED[5]	RED[5]
PIX[86]	DIGITAL RED[6]	RED[6]	RED[6]	RED[6]
PIX[87]	DIGITAL RED[7]	RED[7]	RED[7]	RED[7]
PIX[88]	DIGITAL CLOCK			
PIX[89]	DIGITAL BLANK			

Note 1: The DIGIMODE bits are contained in the Miscellaneous Control 4 register. When DIGIMODE is set to 00 the digital output signals are disabled (high-Z).

Note 2: The digital outputs are shared with VRAM inputs from the high 64 input bits. When the VRAM size is set to 128 the digital outputs are disabled, regardless of the setting of the DIGIMODE bits.

8.0 Power Management

The following registers are used to control power dissipation:

- Power Management (index 0x0005)
- Miscellaneous Clock Control (index 0x0002)
- Sync Control (index 0x0003)
- Miscellaneous Control 1 (index 0x0070)

8.1 DAC Power

The current draw for the analog portion of the DACs can be reduced to a standby current with the DAC PWR bit of the Power Management register.

In addition to the standby current, a small amount of current (approximately 100 µA) will continue to be drawn through the VREFIN input. This can be eliminated if the voltage on VREFIN is reduced to 0 V.

8.2 Driver Power

The power dissipated by the logic output signals can be reduced by 3-stating the drivers. This is done for the SCLK driver by setting the SCLK DSAB bit of the Miscellaneous Clock Control register. The DDOTCLK driver can also be 3-stated by setting the DDOT DSAB bit of the Miscellaneous Clock Control register. HSYNCOUT and VSYNCOUT are 3-stated by setting HSYN CNTL and VSYN CNTL bits of the Sync Control register. The SENSE output is 3-stated by setting the SENS DSAB bit of the Miscellaneous Control 1 register.

The remaining drivers are the microprocessor D[7:0] signals. These are normally 3-stated and will not dissipate power unless a microprocessor read is performed.

8.3 Clocking Power

Most of the digital logic power dissipation occurs as a result of clocking. The ICLK PWR, SCLK PWR, DDOT PWR, and SYNC PWR bits of the Power Management register are used to inhibit the digital logic clocking.

The ICLK PWR bit, when set, inhibits all internal clocking except for the following:

- The PLLs.
- The palette arrays and the cursor array control logic. The clocks to the internal logic are left running because this is required for microprocessor access.
- SCLK and DDOTCLK - The circuitry that generates these clocks is left running in case external components need to run off these clocks.
- The horizontal and vertical sync delay circuits. These circuits are left running to allow sync signals to propagate to the display monitor.

When the ICLK PWR bit is set the DAC outputs will remain stuck at whatever was last clocked into the DACs, unless the DACs are shut down with DAC PWR.

The SCLK PWR bit may be set to disable the clocking to the SCLK generator. The resultant static SCLK output may be left at either the low or high state. As noted above, the SCLK output may be 3-stated with the SCLK DSAB bit of the Miscellaneous Clock Control register.

The DDOT PWR bit may be set to disable the clocking to the DDOTCLK generator. The resultant static DDOTCLK output may be left at either the low or high state. As noted above, the DDOTCLK output may be 3-stated with the DDOT DSAB bit of the Miscellaneous Clock Control register.

The SYNC PWR bit may be set to disable the clocking to the horizontal and vertical sync circuits. These outputs may be left at either the low or high state. (But note that the outputs can be forced high or low or 3-stated with the HSYN CNTL and VSYN CNTL bits of the Sync Control register.)

The starting and stopping of clocks with the SCLK PWR, DDOT PWR, and SYNC PWR bits is asynchronous. Thus, "chopped" pulses may be produced on the SCLK, DDOTCLK, HSYNCOUT and VSYNCOUT outputs when these bits are changed.

Similarly, changing the ICLK PWR bit can disturb the stopping and starting of the internal clocks such that the display is disturbed for a frame. It is recommended that the DACs be blanked with the BLANK CNTL bit of the Miscellaneous Control 2 register before shutting off the clocks, and that a frame be run by after turning on the clocks before the DACs are unblanked again with BLANK CNTL.

8.4 PLL Power

The Pixel PLLs can be shut off with the PLL ENAB bit of the Miscellaneous Clock Control register (Pixel PLL) and the SPLL ENAB bit of the System Clock Control register (SYSCLK PLL). This, in conjunction with turning off the DACs and 3-stating the drivers, produces the lowest power consumption. (The PLLs will continue to draw some standby current.)

Note that in general the Pixel PLL drives SCLK, and the incoming LCLK is generally derived externally from SCLK. If the Pixel PLL is disabled, SCLK will stop running regardless of the setting of SCLK PWR, DDOTCLK will stop running regardless of the setting of DDOT PWR, internal clocking will stop regardless of the setting of ICLK PWR, sync signal clocking will stop regardless of the setting of SYNC PWR, and external circuitry running off SCLK and/or DDOTCLK will stop running.

If EXTCLK is used instead of the PLL the same effect can be achieved by stopping EXTCLK.

9.0 Diagnostic Support

9.1 Data Masks

The Pixel data inputs may be masked by the VRAM Mask registers to diagnose frame buffer problems. Each active bit in the VRAM Mask register controls four bits of the pixel port. Masked bytes introduce zeroes into the data path.

9.2 MISR

The MISR employs a 24-bit shift register with feedback to accumulate a signature of the data presented to the DACs during one screen frame. Signature accumulation is controlled by vertical blanking detection and Miscellaneous Control 1 register bit 7. After MC1(7) changes from '0'b to '1'b, vertical blanking resets the signature to zero at the start of a frame. Signature accumulation ends when vertical blanking goes "on" to end a frame, regardless of the state of MC1(7). The MISR signature can now be read with three cycles from the microprocessor interface. MC1(7) must be written to a '0'b and then a '1'b before a new signature can be generated. In interlace mode, the MISR accumulates one complete frame starting with the ODD field.

9.3 DAC Comparators

Each DAC output is connected to a comparator. Both latched and unlatched copies of the comparator outputs can be read from the DAC Sense register. The logical AND of either the latched or unlatched comparator bits is presented on the $\overline{\text{SENSE}}$ output. The reference inputs of the comparators are connected to the chip CVREF pin. With the internally applied reference voltage of 0.35 V, the corresponding Sense bit will be '1'b when the DAC output is 0 to 0.28 V or '0'b when it is 0.42 V to 0.70 V. These values apply when the DAC is doubly terminated in 75 Ω, RREF=698 Ω, and no sync or blank is present.

10.0 Internal Register - Summary

Table 10 is a summary of the internal registers. Detailed descriptions are given in Section 11.0.

For correct operation, and to preserve upward compatibility, the registers listed as "Reserved" must not be written to. Within a register, individual bits listed as "Reserved" must be set to '0's.

Table 10. Internal Register Summary

RS[2:0]	Index	R/W	Reset Value	Register Name
000	-	✓	U	Palette Address (Write Mode)
001	-	✓	U	Palette Data
010	-	✓	U	Pixel Mask
011	-	✓	U	Palette Address (Read Mode)
100	-	✓	U	Index Low
101	-	✓	U	Index High
110	-	✓	U	Index Data (Indexed Registers)
111	-	✓	U	Index Control
110	0x0000	RO	Rev	Revision Level
110	0x0001	RO	0x02	ID
110	0x0002	✓	0x00	Miscellaneous Clock Control
110	0x0003	✓	0x00	Sync Control
110	0x0004	✓	0x00	Horizontal Sync Position
110	0x0005	✓	0x00	Power Management
110	0x0006	✓	0x00	DAC Operation
110	0x0007	✓	0x00	Palette Control
110	0x0008	✓	0x01	System Clock Control
110	0x0009	-	-	(Reserved)
110	0x000a	✓	U	Pixel Format
110	0x000b	✓	U	8 BPP Control
110	0x000c	✓	U	16 BPP Control
110	0x000d	✓	U	24 BPP Packed Control
110	0x000e	✓	U	32 BPP Control
110	0x000f	✓	U	Buffer A/B Select
110	0x0010	✓	0x00	Pixel PLL Control 1
110	0x0011	✓	0x00	Pixel PLL Control 2
110	0x0012 - 0x0013	-	-	(Reserved)
110	0x0014	✓	U	Fixed Pixel PLL Reference Divider

Table 10. Internal Register Summary (Continued)

RS[2:0]	Index	R/W	Reset Value	Register Name
110	0x0015	✓	0x08	System PLL Reference Divider
110	0x0016	✓	0x41	System PLL VCO Divider
110	0x0017 - 0x001f	-	-	(Reserved)
110	0x0020	✓	0x00	F0 (M0)
110	0x0021	✓	0x00	F1 (N0)
110	0x0022	✓	0x00	F2 (M1)
110	0x0023	✓	0x00	F3 (N1)
110	0x0024	✓	0x00	F4 (M2)
110	0x0025	✓	0x00	F5 (N2)
110	0x0026	✓	0x00	F6 (M3)
110	0x0027	✓	0x00	F7 (N3)
110	0x0028	✓	0x00	F8 (M4)
110	0x0029	✓	0x00	F9 (N4)
110	0x002a	✓	0x00	F10 (M5)
110	0x002b	✓	0x00	F11 (N5)
110	0x002c	✓	0x00	F12 (M6)
110	0x002d	✓	0x00	F13 (N6)
110	0x002e	✓	0x00	F14 (M7)
110	0x002f	✓	0x00	F15 (N7)
110	0x0030	✓	0x00	Cursor Control
110	0x0031	✓	U	Cursor X Low
110	0x0032	✓	U	Cursor X High
110	0x0033	✓	U	Cursor Y Low
110	0x0034	✓	U	Cursor Y High
110	0x0035	✓	U	Cursor Hot Spot X
110	0x0036	✓	U	Cursor Hot Spot Y
110	0x0037 - 0x003f	-	-	(Reserved)
110	0x0040	✓	U	Cursor Color 1 Red
110	0x0041	✓	U	Cursor Color 1 Green
110	0x0042	✓	U	Cursor Color 1 Blue
110	0x0043	✓	U	Cursor Color 2 Red
110	0x0044	✓	U	Cursor Color 2 Green
110	0x0045	✓	U	Cursor Color 2 Blue
110	0x0046	✓	U	Cursor Color 3 Red
110	0x0047	✓	U	Cursor Color 3 Green
110	0x0048	✓	U	Cursor Color 3 Blue
110	0x0049 - 0x005f	-	-	(Reserved)
110	0x0060	✓	U	Border Color Red

Table 10. Internal Register Summary (Continued)

RS[2:0]	Index	R/W	Reset Value	Register Name
110	0x0061	✓	U	Border Color Green
110	0x0062	✓	U	Border Color Blue
110	0x0063 - 0x006f	-	-	(Reserved)
110	0x0070	✓	0x00	Miscellaneous Control 1
110	0x0071	✓	0x00	Miscellaneous Control 2
110	0x0072	✓	0x00	Miscellaneous Control 3
110	0x0073	✓	0x00	Miscellaneous Control 4
110	0x0074 - 0x0081	-	-	(Reserved)
110	0x0082	RO	U	DAC Sense
110	0x0083	-	-	(Reserved)
110	0x0084	RO	U	MISR Red
110	0x0085	-	-	(Reserved)
110	0x0086	RO	U	MISR Green
110	0x0087	-	-	(Reserved)
110	0x0088	RO	U	MISR Blue
110	0x0089 - 0x008d	-	-	(Reserved)
110	0x008e	RO	0x00	Pixel PLL VCO Divider Input
110	0x008f	RO	U	Pixel PLL Reference Divider Input
110	0x0090	✓	U	VRAM Mask 0
110	0x0091	✓	U	VRAM Mask 1
110	0x0092	✓	U	VRAM Mask 2
110	0x0093	✓	U	VRAM Mask 3
110	0x0094 - 0x00ff	-	-	(Reserved)
110	0x0100 - 0x04ff	✓	U	Cursor Array
110	0x0500 0x07ff	-	-	(Reserved)
RO=Read Only, U=Undefined, Rev=Revision Level				

11.0 Register Descriptions

11.1 Direct Access Registers

The direct access registers are addressed using RS[2:0] inputs.

Palette Address (Write Mode)

7	6	5	4	3	2	1	0
WRITE Address							

RS[2:0]: 000
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 WRITE Address - Palette address in write mode.

Operation of this register is discussed in 1.0, "Microprocessor Access," on page 1.

Palette Data

7	6	5	4	3	2	1	0
0	0	Palette Data [7:2]					

7	6	5	4	3	2	1	0
Palette Data [7:0]							

RS[2:0]: 001
Access: Read/Write
Power on Value: Undefined

The format of the palette data depends on the color resolution, 6 or 8 bit.

6 bit color resolution
Miscellaneous Control 2 COL RES = 0

Bits 7 - 6 00
Bits 5 - 0 6 bit palette data

On WRITEs bits 7:6 from the microprocessor are discarded, bits 5:0 are written to bits 7:2 internally, and internal bits 1:0 are set to '00'. On reads internal bits 7:2 are read as bits 5:0, an bits 7:6 are returned as '00'.

8 bit color resolution
Miscellaneous Control 2 COL RES = 1

Bits 7-0 8 bit palette data. Bits 7:0 are written/read internally as bits 7:0

Operation of this register is discussed in 1.0, "Microprocessor Access," on page 1.

Pixel Mask

7	6	5	4	3	2	1	0
Pixel Mask							

RS[2:0]: 010
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Pixel Mask

In indirect color modes this register masks the pixel values used to index into the palettes. Each bit is ANDed with its corresponding pixel bit. A value of 0xff is required to pass the pixel values to the palettes unchanged

The same mask is applied to each of the red, green, and blue pixel addresses into the palettes.

Palette Address (Read Mode) / Palette Access State

7	6	5	4	3	2	1	0
READ Address							

RS[2:0]: 011
Access: Write
Power on Value: -
Bits 7 - 0 READ Address - Palette address in read mode.

7	6	5	4	3	2	1	0
READ Address							

RS[2:0]: 011
Access: Read
Power on Value: Undefined
PADR RFMT: 0
Bits 7 - 0 READ Address - Palette address in read mode.

7	6	5	4	3	2	1	0
Reserved						ACC State	

RS[2:0]: 011
Access: Read
Power on Value: Undefined
PADR RFMT: 1
Bits 7 - 2 Reserved
Bits 1 - 0 ACC STATE - Palette Access State. Reports which mode was used on last write of Palette Address Register.

- 00 Write Mode
- 11 Read Mode

Note that the palette address to be read is written into this register, but the contents that are read depends on the PADR RFMT bit in the Miscellaneous Control 1 register. Operation of these registers is discussed in 1.0, "Microprocessor Access," on page 1.

Index Low

7	6	5	4	3	2	1	0
Index Low							

RS[2:0]: 100
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Index Low

This register, together with Index High, forms the internal index register. It selects the register that will be accessed when the Indexed Data register is written or read.

Index High

7	6	5	4	3	2	1	0
Reserved					Index High		

RS[2:0]: 101
Access: Read/Write
Power on Value: Undefined
Bits 7 - 3 Reserved
Bits 2 - 1 Index High

This register provides the high-order bits of the internal index register.

If auto-increment is turned on, the resulting index is not *defined if an increment past the maximum index value* occurs.

Indexed Data

7	6	5	4	3	2	1	0
Indexed Data							

RS[2:0]: 110

Access: Read/Write

Power on Value: Undefined

Bits 7 - 0 Indexed Data

A write or read to this register will write or read the register addressed by the internal index register (Index High and Index Low).

Following a write or read to Indexed Data, the index register will be incremented if auto-increment is turned on (INDX CNTL bit of the Index Control register).

Index Control

7	6	5	4	3	2	1	0
Reserved							INDX CNTL

RS[2:0]: 111

Access: Read/Write

Power on Value: Undefined

Bits 7 - 1 Reserved

Bit 0 INDX CNTL - Index Control. Controls auto-increment of the index register.

- 0 Off - no auto-increment.
- 1 On - the index register (Index High and Index Low) will increment by one following a write or read to Indexed Data.

11.2 Indexed Registers

The indexed registers are accessed by setting the desired address into the internal index register (Index High and Index Low) and writing or reading the Indexed Data register.

11.2.1 Miscellaneous Control

Miscellaneous Control 1

7	6	5	4	3	2	1	0
MISR CNTL	VMSK CNTL	PADR RFMT	SENS DSAB	SENS SEL	RSVD	VRAM SIZE	

Index: 0x0070

Access: Read/Write

Power on Value: 0x00

Bit 7 MISR CNTL
- 0 Off. If the MISR is running, it will stop at the beginning of the next frame.
- 1 On. The MISR will start accumulating a signature at the start of the next frame (end of vertical blanking).

Bit 6 VMSK CNTL - VRAM Mask Control
- 0 No VRAM masking.
- 1 The VRAM inputs on the PIX[127:00] inputs will be masked under control of the VRAM Mask 0, 1, 2, and 3 registers.

This bit has no effect when the VGA port is selected.

Bit 5 PADR RFMT - Palette Address Register (Read Mode) Format. Specifies the contents returned from the Palette Address register, read mode (RS[2:0] = 011)
- 0 Return the eight bits of the read address
- 1 Return the palette access state in the two low order bits

Bit 4 SENS DSAB - $\overline{\text{SENSE}}$ Driver Disable
- 0 $\overline{\text{SENSE}}$ driver enabled
- 1 $\overline{\text{SENSE}}$ driver disabled (3-stated)

Bit 3 SENS SEL - Sense Select. Selects which bit of the DAC Sense register is presented on the $\overline{\text{SENSE}}$ driver.
- 0 Bit 3 - Unlatched Sense
- 1 Bit 7 - Latched Sense

Bit 2 RSVD - Reserved

Bits 1 - 0 VRAM SIZE - VRAM interface width
- 00 32 bits. PIX[31:0] used, PIX[127:32] ignored.
- 01 64 bits. PIX[63:00] used, PIX[127:64] ignored.
- 10 Reserved
- 11 128 bits. PIX[127:00] used.

These bits have no effect when the VGA port is selected.

Miscellaneous Control 2

7	6	5	4	3	2	1	0
PCLK SEL		INTL MODE	BLANK CNTL	RSVD	COL RES	BRDR/INTL	PORT SEL

Index: 0x0071

Access: Read/Write

Power on Value: 0x00

Bits 7 - 6 PCLK SEL - Pixel Clock Select. Specifies the source of the internal pixel clock.

- 00 LCLK input
- 01 Internal PLL output
- 10 REFCLK input
- 11 Reserved

Note: A selection of 00 (LCLK input) for the pixel clock is required and only valid when PORT SEL = 0 (VGA data inputs), or 32 BPP is selected with a VRAM width of 32.

Bit 5 INTL MODE - Interlace Mode. Controls effect of BORDER/OE input on cursor when this input is used as the ODD/EVEN interlace control.

- 0 Non-interlaced. The BORDER/OE input is ignored.
- 1 Interlaced. If the cursor is turned on, the BORDER/OE input will be used to select display of the odd or even cursor rows.

This bit has no effect when BRDR/INTL (bit 1) is set '0' (BORDER/OE used as BORDER input).

Bit 4 BLANK CNTL - Blanking Control

- 0 Normal operation.
- 1 DACs are blanked. No pixel data is presented on the DACs, but all other operations remain normal, including the collection of a signature if the MISR is turned on.

Bit 3 RSVD - Reserved

Bit 2 COL RES - Color Resolution

- 0 6-bit
- 1 8-bit

With 6-bit color resolution only 6 bits of microprocessor data are loaded into the palettes. Microprocessor data bits D[5:0] are written to/read from palette bits [7:2]. Internally 00 is written to palette bits [1:0], and on reads D[7:6] are forced to 00.

Also with 6-bit color resolution the two low order bits presented from the palettes to the DACs are controlled by Palette Control bit 6BIT LIN.

With 8-bit color resolution all 8 bits from/to the microprocessor are written/read to the palette, and the 8 bits presented to the DACs are unmodified. The 6BIT LIN bit has no effect.

Bit 1 BRDR/INTL - Border/Interlace. Controls usage of BRDR/OE input.

- 0 BORDER/OE input used to indicate "BORDER". (Interlace operation is not supported.)
- 1 BORDER/OE input used to indicate "ODD/EVEN". (Border operation is not supported.)

Bit 0 PORT SEL - Port Select

- 0 VGA Data inputs.
- 1 VRAM pixel port inputs.

Miscellaneous Control 3

7	6	5	4	3	2	1	0
SWAP RB	RSVD	SWAP DWRD	Reserved			SWAP NIB	RSVD

Index: 0x0072

Access: Read/Write

Power on Value: 0x00

Bit 7 SWAP RB - Swap Red and Blue pixel components. In 16, 24, and 32 BPP, this bit causes the red and blue components of the pixels to be swapped. In indirect mode, the swapping takes place before the Palette.

- 0 Normal operation.
- 1 Swap Red and Blue components of the pixel. This bit only has an effect in 16, 24, and 32 BPP.

Bit 6 RSVD - Reserved

Bit 5 SWAP DWRD - Swap incoming double words. With a VRAM width of 128 this bit causes the order of the two incoming double words (8 bytes each) to be swapped.

- 0 Use PIX[63:.00] for first pixels, use PIX[127:63] for next pixels.
- 1 Use PIX[127:63] for first pixels, use PIX[63:00] for next pixels.

Bits 4 - 2 Reserved

Bit 1 SWAP NIB - Swap nibbles within bytes. Used with 4 BPP.

- 0 Use high nibble (e.g., PIX[07:04]) for first pixel, use low nibble (e.g., PIX[03:00]) for next pixel.
- 1 Use low nibble (e.g., PIX[03:00]) for first pixel, use high nibble (e.g., PIX[07:04]) for next pixel.

The same nibble order is applied to each of the incoming bytes. This bit has no effect if the pixel format is not 4 BPP.

Bit 0 Reserved

This register has no effect when the VGA port is selected.

Miscellaneous Control 4

7	6	5	4	3	2	1	0
DIGI MODE		DIGI CDIV	DIGI CINV	BAB UPDT	BAB RDBK	DBL BUF	

Index: 0x0073

Access: Read/Write

Power on Value: 0x00

Bits 7 - 6 DIGI MODE - Digital Interface Mode.

- 00 Digital Interface Disabled
- 01 The 4 most significant bits of the red, green, blue internal pixel values are driven on the 4 most significant bits of red, green, blue digital outputs, with the least significant bits 3-stated.
- 10 The 4 most significant bits of the red, green, blue internal pixel values are driven on the 4 most significant bits of red, green, blue digital outputs and also driven on the 4 least significant bits of the red, green, blue outputs.
- 11 All eight bits of the internal pixel values are driven on the digital outputs.

Note: The DIGI MODE bits only have effect when the VRAM width is *not* set to 128 (Miscellaneous Control 1 register bits 1,0 are *not* set to '11'). If the VRAM width is 128 then the digital interface is disabled.

Bit 5 DIGI CDIV - Digital Interlace Clock Divide.

- 0 Normal clock output.
- 1 The DIGICLK output frequency is divided by 2.

Bit 4 DIGI CINV - Digital Interlace Clock Invert.

- 0 Normal clock output.
- 1 The DIGICLK output is inverted.

Bit 3

BAB UPDT - Buffer A/B Update. Controls when the Buffer A/B register is updated on microprocessor writes to that register.

- 0 Delayed - the Buffer A/B register value is not changed until vertical blanking is detected. At that time, whatever value was last written on the microprocessor interface to the Buffer A/B register will be loaded into that register.
- 1 Immediate - the write will occur immediately.

Bit 2

BAB RDBK - Buffer A/B Readback Value. Selects which value is read on microprocessor reads of the Buffer A/B register.

- 0 Pending - The last value written to the Buffer A/B register from the microprocessor interface. If the BAB UPDT bit is set to 0, a microprocessor write to this register has occurred, and vertical blanking has not yet been detected, the value read back will be the value waiting to be written to the Buffer A/B register, not the actual value in use. If the BAB UPDT is set to 1, or if BAB UPDT is set to 0 and the update has already occurred, then the value read back will be identical to the value in use.
- 1 In use - the value contained in the register, and being used for A/B selection in the current frame.

When the BAB UPDT bit is set to 1 (immediate update) the "pending" and "in use" values are identical, and the same value is read back regardless of the setting of the BAB RDBK bit.

Bits 1 - 0

DBL BUF - Double Buffer Mode Control

- 00 Double Buffer Mode Disabled
- 01 Dual 64-bit buffer - this setting only has effect when the VRAM width is set to 128 bits (Miscellaneous Control 1 register bits 1,0 = '11'). All 128 bits are read in but only 64 bits are used for pixel data; the other 64 bits are discarded. The half that is used for pixels (PIX[63:0] or PIX[127:64] is determined by the BUF A/B bit of the Buffer A/B register. Also, note that SWAP DWRD bit of the Miscellaneous Control 3 register effectively inverts the BUF A/B bit.
- 10 8 BPP double buffer - this setting is valid with any VRAM width. The Pixel Format register must be set to 8 BPP, otherwise setting DBL BUF to '10' will have no effect.

  The timings (e.g., SCLK generation) will be set for 16 BPP operation. But for every 16 bits read from VRAM, only 8 bits will be used for the pixel. The 8 bits selected, low or high, from the 16-bit VRAM data is determined by the BUF A/B bit of the Buffer A/B register. The 8-Bit Pixel Control register determines if indirect or direct color is used.
- 11 Reserved

This register has no effect when the VGA port is selected.

Miscellaneous Clock Control

7	6	5	4	3	2	1	0
DDOT DSAB	SCLK DSAB	B24P DDOT	SCLK INVT	DDOT DIV			PPLL ENAB

Index: 0x0002

Access: Read/Write

Power on Value: 0x00

Bit 7 DDOT DSAB - DDOTCLK driver disable

DDOTCLK driver enabled

- 0 DDOTCLK driver enabled
- 1 DDOTCLK driver disabled (3-stated)

Bit 6 SCLK DSAB - SCLK driver disable

- 0 SCLK driver enabled
- 1 SCLK driver disabled (3-stated)

Bit 5 B24P DDOT - Selects which clock is driven on DDOTCLK when 24 Bit Packed Pixel format is selected.

- 0 Use divided Pixel PLL output under control of DDOT DIV bits.
- 1 Output the same signal as SCLK.

When a format other than 24 BPP Packed is selected, the B24P DDOT bit has no effect and the divided Pixel PLL output is used.

Bit 4 SCLK INVT - Inverts the SCLK output.

Bits 3 - 1 DDOT DIV - DDOTCLK divide factor. Specifies the divide factor applied to the internal Pixel PLL output to produce the DDOTCLK output signal.

- 000 Pixel PLL out/1
- 001 Pixel PLL out/2
- 010 Pixel PLL out/4
- 011 Pixel PLL out/8
- 100 Pixel PLL out/16
- 101 Reserved
- 110 Reserved
- 111 Reserved

Bit 0 PPLL ENAB - Pixel PLL Enable

- 0 Pixel PLL programming disabled.
- 1 Pixel PLL programming enabled.

Sync Control

7	6	5	4	3	2	1	0
DLY CNTL	CSYN INVT	VSYN INVT	HSYN INVT	VSYN CNTL		HSYN CNTL	

Index: 0x0003

Access: Read/Write

Power on Value: 0x00

Bit 7 DLY CNTL - Sync Delay Control. Specifies whether delay matching the pixel pipeline delay should be added to the horizontal sync signal.

- 0 Add matching delay
- 1 Do not add delay

This bit only has effect when the SOG bit of the DAC Operation register is off. If SOG is on (composite sync enabled) then matching pipeline delay is not added to horizontal sync.

Bit 6 CSYN INVT - Invert incoming $\overline{\text{HCSYNCIN}}$ when used as Composite Sync

- 0 Do not invert incoming $\overline{\text{HCSYNCIN}}$
- 1 Invert incoming $\overline{\text{HCSYNCIN}}$

Bit 5 VSYN INVT - Vertical Sync Invert

- 0 Do not invert incoming $\overline{\text{VSYNCIN}}$
- 1 Invert incoming $\overline{\text{VSYNCIN}}$

Bit 4 HSYN INVT - Invert incoming $\overline{\text{HCSYNCIN}}$ when used as Horizontal Sync

- 0 Do not invert incoming $\overline{\text{HCSYNCIN}}$
- 1 Invert incoming $\overline{\text{HCSYNCIN}}$

Bits 3 - 2 VSYN CNTL - Vertical Sync Output Control

- 00 Normal output
- 01 $\overline{\text{VSYNCOUT}}$ forced high
- 10 $\overline{\text{VSYNCOUT}}$ forced low
- 11 $\overline{\text{VSYNCOUT}}$ disabled (3-stated)

Bits 1 - 0 HSYN CNTL - Horizontal Sync Output Control

- 00 Normal output
- 01 $\overline{\text{HSYNCOUT}}$ forced high
- 10 $\overline{\text{HSYNCOUT}}$ forced low
- 11 $\overline{\text{HSYNCOUT}}$ disabled (3-stated)

Horizontal Sync Control

7	6	5	4	3	2	1	0
Reserved				HSYN POS			

Index: 0x0004

Access: Read/Write

Power on Value: 0x00

Bits 7 - 4 Reserved

Bits 3 - 0 HSYN POS - Horizontal Sync Position. Specifies number of additional pixel delays to add to the horizontal sync signal and the composite sync signal.

0000	0 pixels
0001	1 pixel
0010	2 pixels
0011	3 pixels
0100	4 pixels
0101	5 pixels
0110	6 pixels
0111	7 pixels
1000	8 pixels
1001	9 pixels
1010	10 pixels
1011	11 pixels
1100	12 pixels
1101	13 pixels
1110	14 pixels
1111	15 pixels

If the SOG bit of the DAC Operation register is on, the additional pixel delays are added to composite sync. If SOG is off, then the delays are added to horizontal sync, under the control of the DLY CNTL bit of the Sync Control register. (The additional delay specified by the Horizontal Position register will only be added if DLY CNTL is set to 0.)

Power Management

7	6	5	4	3	2	1	0
Reserved			SCLK PWR	DDOT PWR	SYNC PWR	ICLK PWR	DAC PWR

Index: 0x0005

Access: Read/Write

Power on Value: 0x00

Bits 7 - 5 Reserved

Bit 4 SCLK PWR - SCLK Power Control

- 0 Normal Operation
- 1 Disable clocks to SCLK generator

Bit 3 DDOT PWR - DDOTCLK Power Control

- 0 Normal Operation
- 1 Disable clocks to DDOTCLK generator

Bit 2 SYNC PWR - Sync Power Control

- 0 Normal Operation
- 1 Disable clocks to horizontal and vertical sync circuits

Bit 1 ICLK PWR - Internal Clock Power Control

- 0 Normal Operation
- 1 Disable all internal clocks except those for the SCLK generator, DDOTCLK generator, and horizontal and vertical sync circuits.

  A clock is left running to allow microprocessor access of the palette and cursor array, but otherwise the palette and cursor RAMs will not be clocked. The two RAMs will retain their contents.

Bit 0 DAC PWR - DAC Analog Power Control

- 0 Normal Operation
- 1 Disable analog power to the DACs

DAC Operation

7	6	5	4	3	2	1	0
Reserved				SOG	BRB	DSR	DPE

Index: 0x0006

Access: Read/Write

Power on Value: 0x00

Bits 7 - 4 Reserved

Bit 3 SOG - Composite Sync-On-Green
- 0 Sync is disabled on Green DAC.
- 1 Sync is enabled on Green DAC.

Bit 2 BRB - Blank Red and Blue DACs
- 0 Red and Blue DACs have normal function.
- 1 Red and Blue DACs are always blanked.

Bit 1 DSR - DAC Slew Rate

This bit can be written and read, but on the "-A" product revision it has no effect. The DAC slew rate is always fast.

Bit 0 DPE - DAC blanking Pedestal Enable
- 0 Blanking pedestal disabled (0 IRE)
- 1 Blanking pedestal enabled (7.5 IRE)

Palette Control

7	6	5	4	3	2	1	0
6 Bit LIN	Reserved			Partition			

Index: 0x0007

Access: Read/Write

Power on Value: 0x00

Bit 7 6BIT LIN - 6 Bit Linear Color
- 0 Apply linear palette output
- 1 Do not apply linear palette output

This bit only has effect with indirect color modes, and when Color Resolution is set to 6 bits (Miscellaneous Control 2 COL RES bit = 0). For the 8 bits of palette output for each color, the high order two bits 7 and 6 will be substituted for the two low order bits 1 and 0.

Bits 6 - 4 Reserved.

Bits 3 - 0 PALETTE PARTITION - Selects which partition to use within the palettes when the pixel format is either 4 BPP, 15 BPP indirect color, or 16 BPP indirect color.

With 4 BPP the palettes are divided into 16 partitions. Each partition contains 16 entries. Bits 3 - 0 select 1 of the 16 partitions.

With 15 BPP (555) indirect color, the palettes are divided into 8 partitions. Each partition contains 32 entries. Bits 3 - 1 select 1 of the 8 partitions and bit 0 is not used.

With 16 BPP (565) indirect color, the palettes are divided into 4 partitions. Each partition contains 64 entries. All 64 entries of the Green palette are used in each partition. For the Red and Blue palettes only the first 32 entries of each partition are used. Bits 3 - 2 select 1 of the 4 partitions and bits 1 and 0 are not used.

The PARTITION bits have no effect when the pixel format is not 4 BPP, 15 BPP, or 16 BPP. Also, with 15 BPP and 16 BPP the PARTITION bits have no effect unless

1. Indirect color is chosen (16 BPP Control register bits B16 DCOL = 00), AND
2. Contiguous addressing is chosen (16 BPP Control register bit SPR/CNT = 1)

System Clock Control

7	6	5	4	3	2	1	0
RSVD	SYSC DSAB	Reserved				SYSC SRC	SPLL ENAB

Index: 0x0008
Access: Read/Write
Power on Value: 0x01
Bit 7 RSVD - Reserved
Bit 6 SYSC DSAB - SYSCLK driver disable
- 0 SYSCLK driver enabled
- 1 SYSCLK driver disabled (3-stated)

Bits 5 - 2 Reserved
Bit 1 SYSC SRC - SYSCLK output source
- 0 SYSCLK PLL output
- 1 REFCLK input

Bit 0 SPLL ENAB - System PLL enable
- 0 SYSCLK PLL programming disabled
- 1 SYSCLK PLL programming enabled

Buffer A/B Select

7	6	5	4	3	2	1	0
Reserved							BUF A/B

Index: 0x000f
Access: Read/Write
Power on Value: Undefined
Bits 7 - 1 Reserved
Bit 0 BUF A/B - In double buffer modes, selects buffer A or buffer B pixels
- 0 Buffer A
- 1 Buffer B

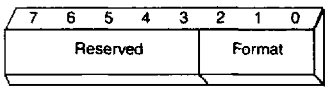
The update time for this register (immediately upon microprocessor write, or wait until vertical blanking detected) is controlled by the BAB UPDT control bit (Miscellaneous Control 4 register bit 3).

The contents that are read back (the microprocessor written value, or the value still retained while waiting for vertical blanking) is controlled by the BAB RDBK control bit (Miscellaneous Control 4 register bit 2).

This register has no effect when double buffer mode is not active (Miscellaneous Control 4 register bits 1,0 = '00').

11.2.2 Pixel Representation

Pixel Format



Index: 0x000a

Access: Read/Write

Power on Value: Undefined

Bits 7 - 3 Reserved

Bits 2 - 0 Pixel Format

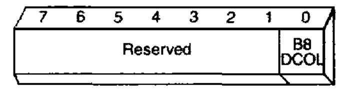
000	Reserved
001	Reserved
010	4 BPP
011	8 BPP
100	15/16 BPP
101	24 BPP Packed
110	32 BPP
111	Reserved

Notes:

1. 4 BPP is not a valid format when the VRAM size is 128. If this register is set to 4 BPP when the VRAM size is 128 (Miscellaneous Control 1 register bits 1,0 = '11') the operation of the chip is undefined.
2. The 24 BPP Packed format requires the VRAM SIZE (Miscellaneous Control 1 register bits 1,0) to be set for 64 or 128 bits. If VRAM SIZE is set to 32 bits then the product operation is undefined if the 24 BPP Packed format is selected.

This register has no effect when the VGA port is selected.

8 Bit Pixel Control



Index: 0x000b

Access: Read/Write

Power on Value: Undefined

Bits 7 - 1 Reserved

Bit 0 B8 DCOL - 8 BPP Direct Color Control

- 0 Indirect Color (through the palette).
- 1 Direct Color (palette bypass). Since the same 8-bit value will be applied to each of the Red, Green, and Blue DACs a monochrome image will be displayed.

This register only affects 8 BPP mode.

16 Bit Pixel Control

7	6	5	4	3	2	1	0
B16 DCOL		BY16 POL	Reserved		ZIB/ LIN	555/ 565	SPR/ CNT

Index: 0x000c

Access: Read/Write

Power on Value: Undefined

Bits 7 - 6 B16 DCOL - 16 BPP Direct Color Control

- 00 Indirect Color (always goes through the palette). Either the 555 or 565 format can be selected. The SPR/CNT bit determines if the access of the palettes is sparse or contiguous. If CNT (contiguous), then the PARTITION bits of the Palette Control register determine which partition of the palettes is used. If SPR (Sparse) the ZIB/ LIN bit must be set to 0 (ZIB).
- 01 Dynamic Bypass. The high order bit of each 16-bit pixel (PIX[15], PIX[31], PIX[47], PIX[63], PIX[79], PIX[95], PIX[111], PIX[127]) is used to select on a pixel-by-pixel basis to either go through the palette (indirect color) or bypass the palette (direct color). When this mode is selected the following conditions apply:
  1. The 555/565 bit has no effect. Internally, the pixel format is forced to 5 bits per color (555).
  2. The SPR/CNT bit has no effect. Internally, sparse addressing (SPR) is forced for palette access.
  3. The ZIB/LIN bit has no effect. Internally, the low order bits for each color are forced to '0's (ZIB) for both access of the palette (indirect color) and palette bypass (direct color).
  4. The Pixel Mask is applied to the pixel data regardless of whether or not the palette is bypassed.
- 10 Reserved
- 11 Direct Color (always bypasses the palette). Either the 555 or 565 format can be selected. The ZIB/LIN bit determines the expansion to 24 bits (low order bit fill). The SPR/CNT bit has no effect.

Bit 5 BY16 POL - Bypass control bit polarity. Determines the meaning of the dynamic bypass control bit (PIX[15], PIX[31], PIX[47], PIX[63], PIX[79], PIX[95], PIX[111], PIX[127]).

0 Control Bit Forces Bypass

Control Bit	***Pixel Path***
0	Through Palette (Indirect Color)
1	Bypass Palette (Direct Color)

1 Control Bit Forces Lookup

Control Bit	***Pixel Path***
0	Bypass Palette (Direct Color)
1	Through Palette (Indirect Color)

The BY16 POL bit has no effect unless the B16 DCOL bits are set to 01.

Bits 4 - 3 Reserved

Bit 2 ZIB/LIN - Bit fill selection. For direct color this bit specifies how the low order bits of each color, R,G,B are filled when 555 or 565 formats are expanded to 24 bits.

- 0 ZIB - Zero Intensity Black. Low order bits are set to 0.
- 1 LIN - Linear. The low order bits are set to the values of the high order bits.

For indirect color if CNT (contiguous) addressing is selected, then ZIB/LIN has no effect. If SPR (sparse) addressing is selected then ZIB/LIN **must** be set to 0 (ZIB). The palette addressing is undefined if LIN bit fill is selected with sparse addressing.

Bit 1 555/565 - Selects 5 bits per color (555) or 5 red, 6 green, 5 blue (565).

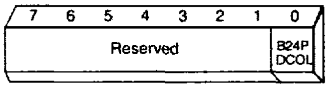
- 0 555
- 1 565

Bit 0 SPR/CNT - Sparse/Continuous. In indirect mode, selects whether index into palette is sparse or contiguous.

- 0 Sparse
- 1 Contiguous

This register only affects 15/16 BPP mode.

24 Bit Packed Pixel Control



Index: 0x000d

Access: Read/Write

Power on Value: Undefined

Bits 7 - 1 Reserved

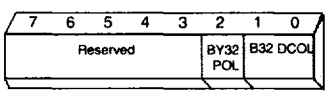
Bit 0 B24P DCOL - 24 BPP Packed Direct Color Control

0 Indirect Color (through the palette).

1 Direct Color (palette bypass).

This register only affects 24 BPP Packed mode.

32 Bit Pixel Control



Index: 0x000e

Access: Read/Write

Power on Value: Undefined

Bit 7 - 3 Reserved

Bit 2 BY32 POL - Bypass control bit polarity. Determines the meaning of the dynamic bypass control bit (PIX[24], PIX[56], PIX[88], PIX[120]).

0 Control Bit Forces Bypass

Control Bit	***Pixel Path***
0	Through Palette (Indirect Color)
1	Bypass Palette (Direct Color)

1 Control Bit Forces Lookup

Control Bit	***Pixel Path***
0	Bypass Palette (Direct Color)
1	Through Palette (Indirect Color)

The BY32 POL bit has no effect unless the B32 DCOL bits are set to 01.

Bits 1 - 0 B32 DCOL - 32 BPP Direct Color Control

00 Indirect Color (always goes through the palette). 24 bits (8 bits each for Red, Green, Blue) are used to index into the palettes. The 8 high order bits (PIX[31:24], PIX[63:56], PIX[95:88], PIX[127:120]) are not used.

01 Dynamic Bypass. A control bit in the high order byte (PIX[24], PIX[56], PIX[88], PIX[120]) is used to select on a pixel-by-pixel basis to either go through the palette (indirect color) or bypass the palette (direct color). The remaining bits in the high order byte (PIX[31:25], PIX[63:57], PIX[95:89], PIX[127:121]) are not used. In this mode, the Pixel Mask is applied to the pixel data regardless of whether or not the palette is bypassed.

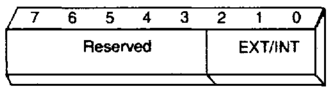
10 Reserved

11 Direct Color (always bypasses the palette). 24 bits (8 bits each for Red, Green, Blue) are presented to the DACs. The 8 high order bits (PIX[31:24], PIX[63:56], PIX[95:88], PIX[127:120]) are not used.

This register only affects 32 BPP mode.

11.2.3 Pixel Clock Frequency Selection

Pixel PLL Control 1



Index: 0x0010

Access: Read/Write

Power on Value: 0x00

Bits 7 - 3 Reserved

Bits 2 - 0 EXT/INT

Determines the source and selection for the Pixel PLL programming registers.

000 External FS[1:0] inputs

One of the F0 - F3 registers is selected with external signals FS[1:0]. The selected register provides the Pixel PLL VCO divider value. The Fixed Pixel PLL Reference Divider register is used to pre-scale the PLL reference clock.

001 External FS[1:0] inputs (4 value M/N programming)

Four pairs of registers M0/N0, M1/N1, M2/N2, M3/N3 are selected with external signals FS[1:0] to provide the VCO divider/reference divider inputs to the Pixel PLL.

The Fixed PLL Reference Divider register is not used.

010 Pixel PLL Control 2 register bits [3:0] (16 value direct programming)

One of the F0 - F15 registers is selected with Pixel PLL Control 2 register bits [3:0]. The selected register provides the Pixel PLL VCO divider value. The Fixed Pixel PLL Reference Divider register is used to prescale the Pixel PLL reference clock.

011 Pixel PLL Control 2 register bits [2:0] (8 value M/N direct programming)

Eight pairs of registers M0/N0, M1/N1, M2/N2, M3/N3, M4/N4, M5/N5, M6/N6, M7/N7 are selected with Pixel PLL Control 2 register bits [2:0] to provide the VCO divider/reference divider inputs to the Pixel PLL.

The Fixed Pixel PLL Reference Divider register is not used. Pixel PLL Control 2 register bit 3 has no effect.

100 Reserved

101 Reserved

110 Reserved

111 Reserved

Pixel PLL Control 2

7	6	5	4	3	2	1	0
Reserved				INT FS			

Index: 0x0011
Access: Read/Write
Power on Value: 0x00
Bits 7 - 3 Reserved
Bits 3 - 0 INT FS - Internal Frequency Selection. Identifies which Pixel PLL programming registers to use when Pixel PLL Control 1 register bits EXT/INT specify internal frequency selection (EXT/INT = 010 or 011).

EXT/INT = 000		EXT/INT = 001	
FS[1:0]	Selected Register	FS[1:0]	Selected Register
00	F0	00	M0, N0
01	F1	01	M1, N1
10	F2	10	M2, N2
11	F3	11	M3, N3

Note: FS[1:0] are the chip inputs FS[1:0]. Pixel PLL Control 2 register is not used when Pixel PLL Control 1 register bits EXT/INT = 000 or 001.

EXT/INT = 010		EXT/INT = 011	
INT FS[3:0]	Selected Register	INT FS[2:0]	Selected Register
0000	F0	000	M0, N0
0001	F1	001	M1, N1
0010	F2	010	M2, N2
0011	F3	011	M3, N3
0100	F4	100	M4, N4
0101	F5	101	M5, N5
0110	F6	110	M6, N6
0111	F7	111	M7, N7
1000	F8		
1001	F9		
1010	F10		
1011	F11		
1100	F12		
1101	F13		
1110	F14		
1111	F15		

Note: When Pixel PLL Control 1 EXT/INT bits = 010 or 011, Pixel PLL Control 2 bits INT FS[3:0] select the frequency register(s). For EXT/INT = 011, INT FS[3] bit is not used and has no effect.

Fixed Pixel PLL Reference Divider

7	6	5	4	3	2	1	0
Reserved			REF DIV COUNT				

Index: 0x0014
Access: Read/Write
Power on Value: Undefined
Bits 7 - 5 Reserved
Bits 4 - 0 REF DIV COUNT - Reference Divide Count

F0-F15: Pixel Frequency 0 to Frequency 15

7	6	5	4	3	2	1	0
DF		VCO DIV COUNT					

Index: 0x0020 - 0x002f
Access: Read/Write
Power on Value: 0x00
Bits 7 - 6 DF - Desired Frequency
Bits 5 - 0 VCO DIV COUNT - VCO Divide Count

The above register diagram shows the format for the 16 pixel frequency registers F0 - F15. This format is selected when the EXT/INT bits (Pixel PLL Control 1 register, bits 2:0) = 000 or 010. The selected F0-F15 register provides the Pixel PLL with the DF value and the VCO divide count. All 16 frequency registers work with the same reference divide count, provided by the Fixed Pixel PLL Reference Divider register.

These 16 registers have a different format (M, N) when EXT/INT = 001 or 011.

M0-M7, N0-N7

7	6	5	4	3	2	1	0
DF		VCO DIV COUNT					

Index: 0x0020, 0x0022, 0x0024, 0x0026, 0x0028, 0x002A, 0x002C, 0x002E
Access: Read/Write
Power on Value: 0x00
Bits 7 - 6 DF - Desired Frequency
Bits 5 - 0 VCO DIV COUNT - VCO Divide Count

7	6	5	4	3	2	1	0
Reserved			REF DIV COUNT				

Index: 0x0021, 0x0023, 0x0025, 0x0027, 0x0029, 0x002B, 0x002D, 0x002F
Access: Read/Write
Power on Value: 0x00
Bits 7 - 5 Reserved
Bits 4 - 0 REF DIV COUNT - Reference Divide Count

The above diagrams show the formats for the 8 'M' and 8 "N" pixel frequency registers. These formats are selected when the EXT/INT bits (Pixel PLL Control 1 Register, bits 2:0) = 001 or 011.

The 8 registers are grouped into four pairs, M0/N0, M1/N1, M2/N2, M3/N3. For a given pair, the "M" register provides the Pixel PLL with the DF value and the VCO divide count, and the "N" register provides the Pixel PLL with the reference divide count.

As described above these 16 registers have a different format (F) when EXT/INT = 000 or 010.

11.2.4 System Clock Frequency Selection

System PLL Reference Divider

7	6	5	4	3	2	1	0
Reserved			REF DIV COUNT				

Index: 0x0015
Access: Read/Write
Power on Value: 0x08
Bits 7 - 5 Reserved
Bits 4 - 0 REF DIV COUNT - Reference Divide Count

System PLL VCO Divider

7	6	5	4	3	2	1	0
DF		VCO DIV COUNT					

Index: 0x0016
Access: Read/Write
Power on Value: 0x41
Bits 7 - 6 DF - Desired Frequency
Bits 5 - 0 VCO DIV COUNT - VCO Divide Count

The System PLL Reference Divider and VCO Divider registers provide the programming values for the system clock (SYSCLK) PLL. The power on values will cause the PLL to produce a SYSCLK frequency of 33 MHz if the incoming reference clock (REFCLK) is 16 MHz.

11.2.5 Cursor

Cursor Control

7	6	5	4	3	2	1	0
SMLC PART		PIX ORDR	LOC READ	UPDT CNTL	CURS SIZE	Cursor Mode	

Index: 0x0030

Access: Read/Write

Power on Value: 0x00

Bits 7 - 6 SMLC PART - Small Cursor Partition. Selects 1 of 4 partitions within the cursor array to use for the 32x32 cursor:

- 00 0x0100 - 0x01ff
- 01 0x0200 - 0x02ff
- 10 0x0300 - 0x03ff
- 11 0x0400 - 0x04ff

These bits have no effect when the cursor size is 64x64.

Bit 5 PIX ORDR - Pixel Order. Specifies ordering of pixel bits in the bytes of the cursor array.

0 Right-to-left

7	6	5	4	3	2	1	0
n+3		n+2		n+1		n+0	

1 Left-to-right

7	6	5	4	3	2	1	0
n+0		n+1		n+2		n+3	

Bit 4 LOC READ - Location Read-back Value. Specifies the value obtained by microprocessor reads of the Cursor X Low, Cursor X High, Cursor Y Low, and Cursor Y High registers.

- 0 Written Value - the value last written.
- 1 Actual Location - the location presently used for display. This will be different than the written value if a location register has been written but the location has not yet been updated. Following a cursor location update the "Written Value" and the "Actual Location" will be the same.

Bit 3 UPDT CNTL - Cursor Location Update Control. Controls when Cursor Location registers are sampled to change the cursor position.

- 0 Delayed - A write to the Cursor Y High register arms the circuitry for the update. The position is then updated (the cursor moves to the new location) when a vertical blanking period is detected.
- 1 Immediate - Move the cursor immediately following a write to any of the Cursor X Low, Cursor X High, Cursor Y Low, or Cursor Y High registers.

Bit 2 Cursor Size

- 0 32x32
- 1 64x64

Bits 1 - 0 Cursor Mode

- 00 OFF
- 01 Mode 0 (3 colors)
- 10 Mode 1 (2 colors and highlighting)
- 11 Mode 2 (2 colors)

Cursor X Low

7	6	5	4	3	2	1	0
Cursor X Low							

Index: 0x0031

Access: Read/Write

Power on Value: Undefined

Bits 7 - 0 Cursor X Low. The low order bits of the cursor X (horizontal) position.

A write to this register will update the cursor position:

1. When both the Cursor Y High register is written and vertical blanking is detected, OR
2. Immediately

under control of the UPDT CNTL bit of the Cursor Control register.

The value read back:

1. Written Value, or
2. Actual Location

is controlled by the LOC READ bit of the Cursor Control register:

Cursor X High

7	6	5	4	3	2	1	0
SIGN	SIGN EXTND			Cursor X High			

Index: 0x0032

Access: Read/Write

Power on Value: Undefined

Bit 7 Sign

Bits 6 - 4 SIGN EXTND - Sign Extended. These bits are always the same as bit 7. On a write these bits are discarded and replaced with the value written to bit 7. On a read they will return the same value as bit 7.

Bits 3 - 0 Cursor X High. The high order bits of the cursor X (horizontal) position.

Cursor X High and Cursor X Low form a combined register that holds a signed cursor X position in two's complement form. The X position range is -4096 to +4095.

A write to this register will update the cursor position:

1. When both the Cursor Y High register is written and vertical blanking is detected, OR
2. Immediately

under control of the UPDT CNTL bit of the Cursor Control register

The value read back:

1. Written Value, or
2. Actual Location

is controlled by the LOC READ bit of the Cursor Control register.

Cursor Y Low

7	6	5	4	3	2	1	0
Cursor Y Low							

Index: 0x0033

Access: Read/Write

Power on Value: Undefined

Bits 7 - 0 Cursor Y Low. The low order bits of the cursor Y (vertical) position.

A write to this register will update the cursor position:

1. When both the Cursor Y High register is written and vertical blanking is detected, or
2. Immediately

under control of the UPDT CNTL bit of the Cursor Control register.

The value read back:

1. Written Value, or
2. Actual Location

is controlled by the LOC READ bit of the Cursor Control register.

Cursor Y High

7	6	5	4	3	2	1	0
SIGN	SIGN EXTND			Cursor Y High			

Index: 0x0034

Access: Read/Write

Power on Value: Undefined

Bit 7 Sign

Bits 6 - 4 SIGN EXTND - Sign Extended. These bits are always the same as bit 7. On a write these bits are discarded and replaced with the value written to bit 7. On a read they will return the same value as bit 7.

Bits 3 - 0 Cursor Y High. The high order bits of the cursor Y (vertical) position.

Cursor Y High and Cursor Y Low form a combined register that holds a signed cursor Y position in two's complement form. The Y position range is -4096 to +4095.

A write to this register will update the cursor position:

1. When vertical blanking is detected, or
2. Immediately

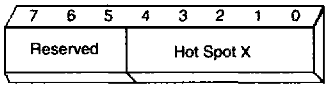
under control of the UPDT CNTL bit of the Cursor Control register.

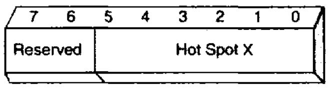
The value read back:

1. Written Value, or
2. Actual Location

is controlled by the LOC READ bit of the Cursor Control register.

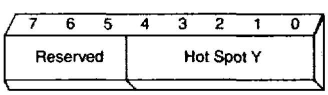
Cursor Hot Spot X

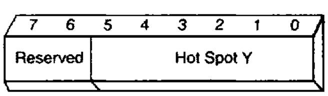




Index: 0x0035
Access: Read/Write
Power on Value: Undefined
32x32 Cursor
Bits 7 - 5 Reserved
Bits 4 - 0 HOT SPOT X. Specifies which pixel in a cursor row is the X position pixel.
64x64 Cursor
Bits 7 - 6 Reserved
Bits 5 - 0 HOT SPOT X. Specifies which pixel in a cursor row is the X position pixel.

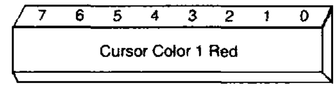
Cursor Hot Spot Y





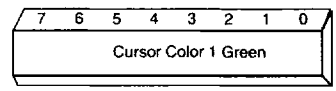
Index: 0x0036
Access: Read/Write
Power on Value: Undefined
32x32 Cursor
Bits 7 - 5 Reserved
Bits 4 - 0 HOT SPOT Y. Specifies which pixel in a cursor column is the Y position pixel.
64x64 Cursor
Bits 7 - 6 Reserved
Bits 5 - 0 HOT SPOT Y. Specifies which pixel in a cursor column is the Y position pixel.

Cursor Color 1 Red



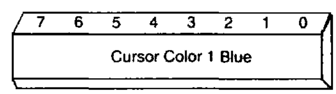
Index: 0x0040
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 1 Red

Cursor Color 1 Green



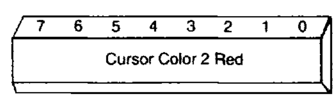
Index: 0x0041
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 1 Green

Cursor Color 1 Blue



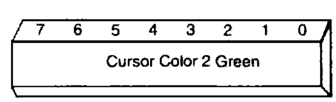
Index: 0x0042
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 1 Blue

Cursor Color 2 Red



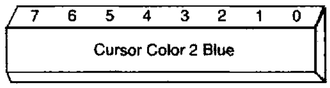
Index: 0x0043
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 2 Red

Cursor Color 2 Green



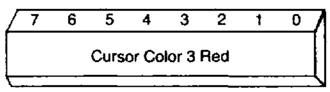
Index: 0x0044
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 2 Green

Cursor Color 2 Blue



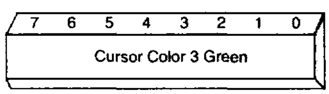
Index: 0x0045
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 2 Blue

Cursor Color 3 Red



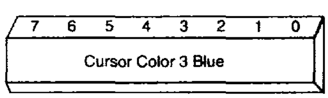
Index: 0x0046
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 3 Red

Cursor Color 3 Green



Index: 0x0047
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 3 Green

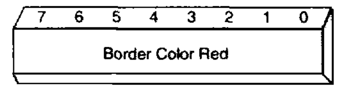
Cursor Color 3 Blue



Index: 0x0048
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Cursor Color 3 Blue

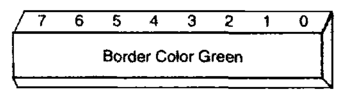
11.2.6 Border Color

Border Color Red



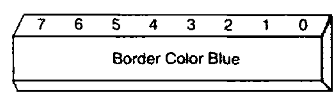
Index: 0x0060
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Border Color Red

Border Color Green



Index: 0x0061
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Border Color Green

Border Color Blue



Index: 0x0062
Access: Read/Write
Power on Value: Undefined
Bits 7 - 0 Border Color Blue

11.2.7 Diagnostic Support

Revision Level

7	6	5	4	3	2	1	0
Revision Level							

Index: 0x0000
Access: Read Only
Power on Value: Revision Level
Bits 7 - 0 Product Revision Level

The value in this register indicates the revision level of the product.

ID

7	6	5	4	3	2	1	0
ID							

Index: 0x0001
Access: Read Only
Power on Value: 0x02
Bits 7 - 0 Product Identification Code

This register distinguishes among the various members of the IBM Microelectronics Palette DAC family. The value of 0x02 indicates that this product is one of several that have two clock generators.

DAC Sense

7	6	5	4	3	2	1	0
LSNS	LBLU COMP	LGRN COMP	LRED COMP	SENS	BLUE COMP	GRN COMP	RED COMP

Index: 0x0082
Access: Read Only
Power on Value: Undefined
Bit 7 LSNS - Latched Sense
Bit 6 LBLU COMP - Latched Blue DAC Comparator Output
Bit 5 LGRN COMP - Latched Green DAC Comparator Output
Bit 4 LRED COMP - Latched Red DAC Comparator Output
Bit 3 SENS - Sense
Bit 2 BLU COMP - Blue DAC Comparator Output
Bit 1 GRN COMP - Green DAC Comparator Output
Bit 0 RED COMP - Red DAC Comparator Output

Bits 2,1,0 are the outputs of the three DAC reference comparators. The DAC output voltages are compared against the 0.35 V internal reference voltage (presented on COMPVREF). These bits are the "raw" outputs of the comparators.

Bits 6,5,4 are latched copies of bits 2,1,0. The latches are clocked during active line time (when BLANK [and BORDER, when a border is used] are both high).

Bit 3 (Sense) represents the combined status of bits 2,1,0. If any of these bits is 0, bit 3 will be 0.

Bit 7 (Latched Sense) represents the combined status of bits 6,5,4. If any of these bits is 0, bit 7 will be 0.

Either bit 3 or bit 7 will be presented on the SENSE output, depending on the SENS SEL bit of the Miscellaneous Control 1 register.

If the selected bit is 0, SENSE will be low.
If the selected bit is 1, SENSE will be high.

MISR Red

7	6	5	4	3	2	1	0
MISR Red							

Index: 0x0084
Access: Read Only
Power on Value: Undefined
Bits 7 - 0 Multiple Input Signature Register Red

This register along with MISR GREEN and MISR BLUE is used to accumulate a diagnostic signature on the values presented to the DACs. The input to the Red DAC is the parallel data input to this portion of the MISR.

MISR Green

7	6	5	4	3	2	1	0
MISR Green							

Index: 0x0086
Access: Read Only
Power on Value: Undefined
Bits 7 - 0 Multiple Input Signature Register Green

This register along with MISR RED and MISR BLUE is used to accumulate a diagnostic signature on the values presented to the DACs. The input to the Green DAC is the parallel data input to this portion of the MISR.

MISR Blue

7	6	5	4	3	2	1	0
MISR Blue							

Index: 0x0088
Access: Read Only
Power on Value: Undefined
Bits 7 - 0 Multiple Input Signature Register Blue

This register along with MISR RED and MISR GREEN is used to accumulate a diagnostic signature on the values presented to the DACs. The input to the Blue DAC is the parallel data input to this portion of the MISR.

Note: The reset, accumulation, and hold function of the MISR is controlled by the MISR CNTL bit of the Miscellaneous Control 1 register, and the $\overline{\text{BLANK}}$ input. See 9.0, "Diagnostic Support," on page 30 for more information.

PLL VCO Divider Input

7	6	5	4	3	2	1	0
DF		VCO DIV COUNT					

Index: 0x008e
Access: Read Only
Power on Value: 0x00
Bits 7 - 6 DF - Desired Frequency
Bits 5 - 0 VCO DIV COUNT - VCO Divide Count

This register allows readback of the selected PLL VCO divider input. It is one of these registers:

- F0, F1, F2, F3, F4, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15
- M0, M1, M2, M3, M4, M5, M6, M7

as determined by the PLL Control 1 EXT/INT bits (2:0), the inputs FS[3:0], and PLL Control 2 INT FS bits (3:0).

PLL Reference Divider Input

7	6	5	4	3	2	1	0
Reserved			REF DIV COUNT				

Index: 0x008f
Access: Read Only
Power on Value: Undefined
Bits 7 - 5 Reserved
Bits 4 - 0 REF DIV COUNT - Reference Divide Count

This register allows readback of the input to the PLL reference divider.

- Fixed PLL Reference Divider
- N0, N1, N2, N3, N4, N5, N6, N7

as determined by the PLL Control 1 EXT/INT bits (2:0), the inputs FS[3:0], and PLL Control 2 INT FS bits (3:0).

VRAM Mask 0

7	6	5	4	3	2	1	0
MASK 31:28	MASK 27:24	MASK 23:20	MASK 19:16	MASK 15:12	MASK 11:08	MASK 07:04	MASK 03:00

Index: 0x0090
Access: Read/Write
Power on Value: Undefined

Bit 7 Mask VRAM PIX inputs 31:28
Bit 6 Mask VRAM PIX inputs 27:24
Bit 5 Mask VRAM PIX inputs 23:20
Bit 4 Mask VRAM PIX inputs 19:16
Bit 3 Mask VRAM PIX inputs 15:12
Bit 2 Mask VRAM PIX inputs 11:08
Bit 1 Mask VRAM PIX inputs 07:04
Bit 0 Mask VRAM PIX inputs 03:00

A value of 1 on any of the bits in this register masks (forces to 0) the corresponding received VRAM pixel port inputs. This register has no effect on the inputs unless enabled with the VMSK CNTL bit of the Miscellaneous Control 1 register.

VRAM Mask 1

7	6	5	4	3	2	1	0
MASK 63:60	MASK 59:56	MASK 55:52	MASK 51:48	MASK 47:44	MASK 43:40	MASK 39:36	MASK 35:32

Index: 0x0091
Access: Read/Write
Power on Value: Undefined

Bit 7 Mask VRAM PIX inputs 63:60
Bit 6 Mask VRAM PIX inputs 59:56
Bit 5 Mask VRAM PIX inputs 55:52
Bit 4 Mask VRAM PIX inputs 51:48
Bit 3 Mask VRAM PIX inputs 47:44
Bit 2 Mask VRAM PIX inputs 43:40
Bit 1 Mask VRAM PIX inputs 39:36
Bit 0 Mask VRAM PIX inputs 35:32

A value of 1 on any of the bits in this register masks (forces to 0) the corresponding received VRAM pixel port inputs. This register has no effect on the inputs unless enabled with the VMSK CNTL bit of the Miscellaneous Control 1 register.

VRAM Mask 2

7	6	5	4	3	2	1	0
MASK 95:92	MASK 91:98	MASK 87:84	MASK 83:80	MASK 79:76	MASK 75:72	MASK 71:68	MASK 67:64

Index: 0x0092
Access: Read/Write
Power on Value: Undefined

Bit 7 Mask VRAM PIX inputs 95:92
Bit 6 Mask VRAM PIX inputs 91:88
Bit 5 Mask VRAM PIX inputs 87:84
Bit 4 Mask VRAM PIX inputs 83:80
Bit 3 Mask VRAM PIX inputs 79:76
Bit 2 Mask VRAM PIX inputs 75:72
Bit 1 Mask VRAM PIX inputs 71:68
Bit 0 Mask VRAM PIX inputs 67:64

A value of 1 on any of the bits in this register masks (forces to 0) the corresponding received VRAM pixel port inputs. This register has no effect on the inputs unless enabled with the VMSK CNTL bit of the Miscellaneous Control 1 register.

VRAM Mask 3

7	6	5	4	3	2	1	0
MASK 127:124	MASK 123:120	MASK 119:116	MASK 115:112	MASK 111:108	MASK 107:104	MASK 103:100	MASK 99:96

Index: 0x0093
Access: Read/Write
Power on Value: Undefined

Bit 7 Mask VRAM PIX inputs 127:124
Bit 6 Mask VRAM PIX inputs 123:120
Bit 5 Mask VRAM PIX inputs 119:116
Bit 4 Mask VRAM PIX inputs 115:112
Bit 3 Mask VRAM PIX inputs 111:108
Bit 2 Mask VRAM PIX inputs 107:104
Bit 1 Mask VRAM PIX inputs 103:100
Bit 0 Mask VRAM PIX inputs 99:96

A value of 1 on any of the bits in this register masks (forces to 0) the corresponding received VRAM pixel port inputs. This register has no effect on the inputs unless enabled with the VMSK CNTL bit of the Miscellaneous Control 1 register.

Note: The mask function is intended to be used with the MISR for diagnostics. See 9.0, "Diagnostic Support," on page 30 for more details.

12.0 Pin Descriptions

Table 11. Pin Descriptions

Signal	Type	Pin(s)	Description
Clocks and Clock Controls			
REFCLK	I	117	Reference Clock. A fixed frequency of 2 MHz to 100 MHz applied to this pin provides the reference clock for the programmable pixel and system clock PLLs. When the Direct Programming method is used the REFCLK frequency range is 4 MHz to 62 MHz on 2 MHz boundaries.
FS[1:0]	I	134,120	Frequency Select. These two inputs select one of four sets of registers containing the programming values for the pixel PLL.
DDOTCLK	O	158	Divided Dot Clock. The output of the pixel PLL, divided by 1, 2, 4, 8 or 16. The divide factor is under register control. In 24 BPP Packed pixel mode the SCLK signal can be selected for this output instead of the divided pixel PLL output, under register control. This output can be 3-stated under register control.
SCLK	O	154	Serial Clock. A divided version of the pixel PLL, where the divide ratio is determined by the required bandwidth of the incoming pixels. When the PIX port is selected, the SCLK frequency is a function of the VRAM width and the pixel format (bits per pixel). SCLK is equal to the pixel PLL output when the VGA port is selected. This output can be 3-stated under register control.
LCLK	I	147	Load Clock. Latches data from the PIX port, the VGA port, and the video control inputs.
SYSCLK	O	112	System Clock. The output of the SYSCLK programmable PLL. Also the REFCLK input can be steered to this output. This output can be 3-stated under register control.
Type: I = Input, O = Output, B = Bidirectional, C = Component			

Table 11. Pin Descriptions (Continued)

Signal	Type	Pin(s)	Description
Video Data Inputs			
PIX[63:0]	I	17,16,15,14,98,97,96,95, 165,164,163,162,161,160, 159,208,207,206,205,204, 203,202,201,106,102,101, 100,99,13,12,11,10,9,8,7, 6,173,172,171,170,169, 168,167,166,82,81,80,79, 78,76,90,74,73,89,71,88, 87,86,85,66,65,84,75,62	Pixel data in from VRAMs, low 64 bits. Pixel data in can be selected as 128, 64 or 32 bits using the VRAM SIZE bits of the Miscellaneous Control 1 register. For 32-bit use inputs PIX[63:32] are not used. Latched on rising edge of LCLK. These pins are not shared.
PIX[89:64] & Digital Output	I/O	200,199,198,197,196,195, 194,193,192,191,190,189, 188,187,186,185,184, 182,181,180,179,178,177, 176,175,174 (*)	These pins are shared, and serve either as pixel data in or digital data out. When the VRAM size is set to 128 these pins are pixel data in from VRAMs. When the VRAM size is set to 64 or 32, and the digital outputs are enabled (using the DIGI MODE bits of the Miscellaneous Control 4 register), these pins will be outputs for the digital data. Otherwise they will be unused. When used as VRAM data these inputs are latched on rising edge of LCLK.
PIX[119:90]	I	53,52,48,47,21,20,19,18, 83,72,70,69,68,67. 64,63,94,93,92,91, 5,4,153,152,151, 111,110,109,108,107	Pixel data in from VRAMs. These inputs are only used when the VRAM size is 128. Latched on rising edge of LCLK. These pins are not shared.
PIX[127:120] & VGA[7:0]	I	61,60,59,58,57,56,55,54	These pins are shared, and serve either as VRAM pixel data in or VGA pixel data in. When the VRAM size is 64 or 32 (not 128), then these pins may be used exclusively for VGA pixel data. When the VRAM size is set to 128, then the usage of these pins, as either VGA data or VRAM data, is determined by the PORT SEL (port select) bit of the Miscellaneous Control 2 register. For both uses, the pixel data is latched on the rising edge of LCLK.
		(*) Note that pins 200:174 are shared with digital data out, as listed under the heading "Digital Pixel Outputs" on page 63.	
Type: I = Input, O = Output, B = Bidirectional, C = Component			

Table 11. Pin Descriptions (Continued)

Signal	Type	Pin(s)	Description
Video Control Inputs			
BLANK	I	115	A low level indicates blanking time; a high level indicates active picture time (pixel data, cursor, or border displayed). Latched on rising edge of LCLK.
BORDER/OE	I	116	This is a shared input. It may be used either as a border indicator, or as an interlace control. Within this document, this input may be referred to as BORDER or ODD/EVEN, depending on usage. When used as BORDER: When BLANK is high (picture time), a low level on BORDER indicates the contents of the border registers should be displayed, and a high level indicates that pixel data or cursor should be displayed. When BLANK is low (blanking time) BORDER must be low. If no border is to be displayed BORDER should be tied to BLANK. Latched on rising edge of LCLK. When used as O/E (ODD/EVEN): Used in interlace mode to identify a field as odd or even; determines which row of cursor RAM to display if the cursor is enabled. In this usage the input should only change during vertical blanking.
HCSYNCIN	I	114	This is a shared input. It may be used either as horizontal sync in or composite sync in. When used as Horizontal Sync In, a delayed copy of this signal is presented on HSYNCOUT to align the timing of horizontal sync to the pixel data at the DACs. The incoming polarity can be inverted under register control. Latched on rising edge of LCLK. When used as Composite Sync In, when enabled, this signal is presented on the Green DAC with the video data. The signal is delayed to match the delay of the pixel data. The incoming polarity can be inverted under register control. Latched on rising edge of LCLK
VSYNCIN	I	113	Vertical Sync In. A copy of this signal is presented on VSYNCOUT. The incoming polarity can be inverted under register control.
Video Control Outputs			
HSYNCOUT	O	46	Horizontal Sync Out. This is a copy of HCSYNCIN (or inverted HCSYNCIN), delayed by the same number of pixel clocks as seen by the pixel data at the input to the DACs. It can be forced to a high or low level or 3-stated under register control. The amount of delay may also be adjusted with the Horizontal Sync Position register.
VSYNCOUT	O	23	Vertical Sync Out. This is a copy of VSYNCIN (or inverted VSYNCIN). It can be forced to a high or low level or 3-stated under register control.
Type: I = Input, O = Output, B = Bidirectional, C = Component			

Table 11. Pin Descriptions (Continued)

Signal	Type	Pin(s)	Description
Microprocessor Interface			
$\overline{WR}$	I	141	Write strobe. Writes data into the register selected by RS[2:0] The leading edge samples RS[2:0]. The trailing edge clocks the data on D[7:0] into the selected register.
$\overline{RD}$	I	140	Read strobe. Drives the register contents selected by RS[2:0] onto D[7:0]. The leading edge samples RS[2:0]. When $\overline{RD}$ is low the D[7:0] drivers are enabled.
RS[2:0]	I	139,138,137	Register selects. Sampled on the leading edge of $\overline{WR}$ and $\overline{RD}$ and used to select one of the direct access registers. See Direct Access Registers for more details.
D[7:0]	B	150,149,148,146, 145,144,143,142	Bidirectional data bus for internal register write and read data. The drivers are enabled when $\overline{RD}$ is low, otherwise they are 3-stated.
Miscellaneous			
$\overline{RESET}$	I	118	Internal register and PLL reset. Resets bits of certain registers to a given state. (Generally set to VGA operation. See register descriptions for details.) Also initializes PLL circuits. A reset is **required** following power on to guarantee proper PLL operation.
VGAMODE	O	136	Indicates the VGA port is the selected pixel port. This output is the inverted state of Miscellaneous Control 2 register bit 0 (PORT SEL).
$\overline{SENSE}$	O	22	DAC sense comparator output. Goes low when one or more of the three DAC outputs is above the comparator voltage reference. The three individual comparator outputs are also available as register bits. Either unlatched or latched comparator outputs may be selected for generating the $\overline{SENSE}$ output, under register control. This output can be 3-stated under register control.
Video Outputs			
RED	O	31	Plus RED video out.
$\overline{RED}$	O	34	Minus RED video out.
GREEN	O	40	Plus GREEN video out.
$\overline{GREEN}$	O	41	Minus GREEN video out.
BLUE	O	44	Plus BLUE video out.
$\overline{BLUE}$	O	43	Minus BLUE video out.

Type: I = Input, O = Output, B = Bidirectional, C = Component

Table 11. Pin Descriptions (Continued)

Signal	Type	Pin(s)	Description
			Digital Pixel Outputs
DIGICLK	I/O	199 (*)	This pin is shared, and serves either as pixel data in or digital data clock out. When used as digital data clock out, the default is for the rising edge of the clock to indicate valid data on the DIGIRED, DIGIGRN, and DIGIBLU outputs. The clock can be inverted under register control to use the negative edge. The clock can also be set to run at half frequency to use the rising edge for one pixel and the negative edge for the next pixel.
DIGIBLK	I/O	200 (*)	This pin is shared, and serves either as pixel data in or digital data blank out. When used as digital data blank out, the DIGIBLK output is the same signal as the $\overline{\text{BLANK}}$ input, inverted, delayed to match the internal pixel delay and synchronized with DIGICLK.
DIGIRED[7:0]	I/O	198,197,196,195, 194,193,192,191 (*)	These pins are shared, and serve either as pixel data in or digital data out. When used as digital data out, these pins are the red pixel bits.
DIGIGRN[7:0]	I/O	190,189,188,187, 186,185,184,182 (*)	These pins are shared, and serve either as pixel data in or digital data out. When used as digital data out, these pins are the green pixel bits.
DIGIBLU[7:0]	I/O	181,180,179,178, 177,176,175,174 (*)	These pins are shared, and serve either as pixel data in or digital data out. When used as digital data out, these pins are the blue pixel bits.
		(*) Note that pins 200:174 are shared with VRAM PIX[89:64], as listed under the heading "Video Data Inputs" on page 60.	
Type: I = Input, O = Output, B = Bidirectional, C = Component			

Table 11. Pin Descriptions (Continued)

Signal	Type	Pin(s)	Description
DAC Support			
VREFIN	C	29	Voltage Reference In for the DACs. Connect 1.235 V to this pin and decouple it with a 10 nF ceramic capacitor to DACGND.
RREF	C	38	Resistor Reference. Connect a resistor from this pin to DACGND. This pin connects to an internal op amp which compares the voltage on this pin to that of VREFIN, and adjusts the current flowing out of the RREF pin such that the voltage developed across the reference resistor matches VREFIN. The value of the resistor determines the full scale output current of the DACs. A value of 698 Ω is recommended.
CVREF	C	26	Comparator Voltage Reference. An internal voltage divider between VREFIN and DACGND sets this pin to 0.35V. It is used internally by comparators to sense the values of the DAC outputs. Decouple this pin to DACGND with a 1nF ceramic capacitor.
GREF	C	25	DAC Gate Reference. Output of DAC op amp and input to gates of devices connecting DACVDD to the DAC current switches. Decouple this pin to DACVDD with a 1 nF ceramic capacitor.
PLL Support			
RCI0	C	130	Pixel PLL Loop filter. Connect to parallel 1.3 KΩ resistor and 680 pF capacitor. Return parallel resistor and capacitor to RCRET0 through 8.2 nF capacitor.
RCRET0	C	129	Pixel PLL Loop filter return. Connect as described above under RCI0.
RCI1	C	125	SYSCLK PLL Loop filter. Connect to parallel 1.3 KΩ resistor and 680 pF capacitor. Return parallel resistor and capacitor to RCRET1 through 8.2 nF capacitor.
RCRET1	C	124	SYSCLK PLL Loop filter return. Connect as described above under RCI1.
Type: I = Input, O = Output, B = Bidirectional, C = Component			

Table 11. Pin Descriptions (Continued)

Signal	Type	Pin(s)	Description
			Manufacturing Test
TESTMODE	I	132	This input must be low for functional use. Leave it unconnected. An internal pulldown resistor causes this input to be at ground level.
$\overline{\text{DI1}}$	I	121	This input must be high for functional use.
$\overline{\text{DI2}}$	I	123	This input must be high for functional use.
$\overline{\text{RI}}$	I	133	This input must be high for functional use. An external 1 KΩ resistor to VDD is recommended.
			Power and Ground
VDD		1,3,49,51,103,105,155, 157	Logic Power (3.3 V)
GND		2,28,50,77,104,119,135, 156,183	Logic Ground
DACVDD		24,30,32,36,39,45	DAC Power (3.3 V)
DACGND		27,33,35,37,42	DAC Ground
PLLVDD		128,131	PLL Power (3.3 V)
PLLGND		126,127	PLL Ground
			Unused
NC		122	No Connect. These pins must be left unconnected.
Type: I = Input, O = Output, B = Bidirectional, C = Component			

Table 12. Signal List by Pin Number

Pin	Signal	Description
001	VDD	Logic Power (+3.3 V)
002	GND	Logic Ground
003	VDD	Logic Power (+3.3 V)
004	PIX[98]	Pixel Data In
005	PIX[99]	Pixel Data In
006	PIX[28]	Pixel Data In
007	PIX[29]	Pixel Data In
008	PIX[30]	Pixel Data In
009	PIX[31]	Pixel Data In
010	PIX[32]	Pixel Data In
011	PIX[33]	Pixel Data In
012	PIX[34]	Pixel Data In
013	PIX[35]	Pixel Data In
014	PIX[60]	Pixel Data In
015	PIX[61]	Pixel Data In
016	PIX[62]	Pixel Data In
017	PIX[63]	Pixel Data In
018	PIX[112]	Pixel Data In
019	PIX[113]	Pixel Data In
020	PIX[114]	Pixel Data In
021	PIX[115]	Pixel Data In
022	SENSE	DAC Sense
023	VSYNCOUT	Vertical Sync Out
024	DACVDD	DAC Power (+3.3V)
025	GREF	DAC Gate Ref
026	CVREF	DAC Comp. VREF
027	DACGND	DAC Ground
028	GND	Logic Ground
029	VREFIN	DAC Voltage Ref
030	DACVDD	DAC Power (+3.3V)
031	RED	+ Red Output
032	DACVDD	DAC Power (+3.3V)
033	DACGND	DAC Ground
034	RED	- Red Output
035	DACGND	DAC Ground
036	DACVDD	DAC Power (+3.3V)
037	DACGND	DAC Ground
038	RREF	DAC Resistor Ref
039	DACVDD	DAC Power (+3.3V)
040	GREEN	+ Green Output
041	GREEN	- Green Output
042	DACGND	DAC Ground
043	BLUE	- Blue Output
044	BLUE	+ Blue Output
045	DACVDD	DAC Power (+3.3V)
046	HSYNCOUT	Horizontal Sync Out
047	PIX[116]	Pixel Data In
048	PIX[117]	Pixel Data In
049	VDD	Logic Power (+3.3 V)
050	GND	Logic Ground
051	VDD	Logic Power (+3.3 V)
052	PIX[118]	Pixel Data In
053	PIX[119]	Pixel Data In
054	PX[120]/V[0]	Pixel/VGA Data In
055	PX[121]/V[1]	Pixel/VGA Data In
056	PX[122]/V[2]	Pixel/VGA Data In
057	PX[123]/V[3]	Pixel/VGA Data In
058	PX[124]/V[4]	Pixel/VGA Data In
059	PX[125]/V[5]	Pixel/VGA Data In
060	PX[126]/V[6]	Pixel/VGA Data In
061	PX[127]/V[7]	Pixel/VGA Data In
062	PIX[0]	Pixel Data In
063	PIX[104]	Pixel Data In
064	PIX[105]	Pixel Data In
065	PIX[3]	Pixel Data In
066	PIX[4]	Pixel Data In
067	PIX[106]	Pixel Data In
068	PIX[107]	Pixel Data In
069	PIX[108]	Pixel Data In
070	PIX[109]	Pixel Data In
071	PIX[9]	Pixel Data In
072	PIX[110]	Pixel Data In
073	PIX[11]	Pixel Data In
074	PIX[12]	Pixel Data In
075	PIX[1]	Pixel Data In
076	PIX[14]	Pixel Data In
077	GND	Logic Ground
078	PIX[15]	Pixel Data In
079	PIX[16]	Pixel Data In
080	PIX[17]	Pixel Data In
081	PIX[18]	Pixel Data In
082	PIX[19]	Pixel Data In
083	PIX[111]	Pixel Data In
084	PIX[2]	Pixel Data In
085	PIX[5]	Pixel Data In
086	PIX[6]	Pixel Data In
087	PIX[7]	Pixel Data In
088	PIX[8]	Pixel Data In
089	PIX[10]	Pixel Data In
090	PIX[13]	Pixel Data In
091	PIX[100]	Pixel Data In
092	PIX[101]	Pixel Data In
093	PIX[102]	Pixel Data In
094	PIX[103]	Pixel Data In
095	PIX[56]	Pixel Data In
096	PIX[57]	Pixel Data In
097	PIX[58]	Pixel Data In
098	PIX[59]	Pixel Data In
099	PIX[36]	Pixel Data In
100	PIX[37]	Pixel Data In
101	PIX[38]	Pixel Data In
102	PIX[39]	Pixel Data In
103	VDD	Logic Power (+3.3 V)
104	GND	Logic Ground
105	VDD	Logic Power (+3.3 V)
106	PIX[40]	Pixel Data In
107	PIX[90]	Pixel Data In
108	PIX[91]	Pixel Data In
109	PIX[92]	Pixel Data In
110	PIX[93]	Pixel Data In
111	PIX[94]	Pixel Data In
112	SYSCLK	System Clock Out
113	VSYNCIN	Vertical Sync In
114	HCSYNCIN	Hor/Comp Sync In
115	BLANK	Blank In
116	BORDER/OE	Border/Interlace In
117	REFCLK	PLL Ref. Clock In
118	RESET	Reset
119	GND	Logic Ground
120	FS[0]	Frequency Select
121	DI1	Driver Inhibit 1 (Test)
122	NC	No Connect
123	DI2	Driver Inhibit 2 (Test)
124	RCRET1	Sys Loop Filter Rtrn
125	RCI1	Sys Loop Filter
126	PLLGND	PLL Ground
127	PLLGND	PLL Ground
128	PLLVDD	PLL Power (+3.3V)
129	RCRET0	Pix Loop Filter Rtrn
130	RCI0	Pix Loop Filter
131	PLLVDD	PLL Power (+3.3V)
132	TESTMODE	Test Mode (Test)
133	RI	Receiver Inhibit (Test)
134	FS[1]	Frequency Select
135	GND	Logic Ground
136	VGAMODE	VGA Mode Out
137	RS[0]	Register Select [0]
138	RS[1]	Register Select [1]
139	RS[2]	Register Select [2]
140	RD	Microprocessor Read
141	WR	Microprocessor Write
142	D[0]	Microprocessor Data
143	D[1]	Microprocessor Data
144	D[2]	Microprocessor Data
145	D[3]	Microprocessor Data
146	D[4]	Microprocessor Data
147	LCLK	Load Clock In
148	D[5]	Microprocessor Data
149	D[6]	Microprocessor Data
150	D[7]	Microprocessor Data
151	PIX[95]	Pixel Data In
152	PIX[96]	Pixel Data In
153	PIX[97]	Pixel Data In
154	SCLK	Serial Clock Out
155	VDD	Logic Power (+3.3 V)
156	GND	Logic Ground
157	VDD	Logic Power (+3.3 V)
158	DDOTCLK	Divided Dot Clock Out
159	PIX[49]	Pixel Data In
160	PIX[50]	Pixel Data In
161	PIX[51]	Pixel Data In
162	PIX[52]	Pixel Data In
163	PIX[53]	Pixel Data In
164	PIX[54]	Pixel Data In
165	PIX[55]	Pixel Data In
166	PIX[20]	Pixel Data In
167	PIX[21]	Pixel Data In
168	PIX[22]	Pixel Data In
169	PIX[23]	Pixel Data In
170	PIX[24]	Pixel Data In
171	PIX[25]	Pixel Data In
172	PIX[26]	Pixel Data In
173	PIX[27]	Pixel Data In
174	PX[64]/DB[0]	Pixel In/DigiBlu Out
175	PX[65]/DB[1]	Pixel In/DigiBlu Out
176	PX[66]/DB[2]	Pixel In/DigiBlu Out
177	PX[67]/DB[3]	Pixel In/DigiBlu Out
178	PX[68]/DB[4]	Pixel In/DigiBlu Out
179	PX[69]/DB[5]	Pixel In/DigiBlu Out
180	PX[70]/DB[6]	Pixel In/DigiBlu Out
181	PX[71]/DB[7]	Pixel In/DigiBlu Out
182	PX[72]/DG[0]	Pixel In/DigiGrn Out
183	GND	Logic Ground
184	PX[73]/DG[1]	Pixel In/DigiGrn Out
185	PX[74]/DG[2]	Pixel In/DigiGrn Out
186	PX[75]/DG[3]	Pixel In/DigiGrn Out
187	PX[76]/DG[4]	Pixel In/DigiGrn Out
188	PX[77]/DG[5]	Pixel In/DigiGrn Out
189	PX[78]/DG[6]	Pixel In/DigiGrn Out
190	PX[79]/DG[7]	Pixel In/DigiGrn Out
191	PX[80]/DR[0]	Pixel In/DigiRed Out
192	PX[81]/DR[1]	Pixel In/DigiRed Out
193	PX[82]/DR[2]	Pixel In/DigiRed Out
194	PX[83]/DR[3]	Pixel In/DigiRed Out
195	PX[84]/DR[4]	Pixel In/DigiRed Out
196	PX[85]/DR[5]	Pixel In/DigiRed Out
197	PX[86]/DR[6]	Pixel In/DigiRed Out
198	PX[87]/DR[7]	Pixel In/DigiRed Out
199	PX[88]/DCLK	Pixel In/DigiClk Out
200	PX[89]/DBLK	Pixel In/DigiBlnk Out
201	PIX[41]	Pixel Data In
202	PIX[42]	Pixel Data In
203	PIX[43]	Pixel Data In
204	PIX[44]	Pixel Data In
205	PIX[45]	Pixel Data In
206	PIX[46]	Pixel Data In
207	PIX[47]	Pixel Data In
208	PIX[48]	Pixel Data In

13.0 Electrical and Timing Specifications

Table 13. Recommended Operating Conditions

Parameter	Symbol	170 MHz		220 MHz		250 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Power Supply	VDD, DACVDD, PLLVDD	3.0	3.6	3.0	3.6	3.42	3.78	Volts
Case Temperature	T_C	0	100	0	100	0	100	°C
DAC Output Load	R_L	37.5	50	37.5	50	37.5	50	Ω
Reference Voltage	V_{REF}	1.204	1.266	1.204	1.266	1.204	1.266	Volts

Table 14. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Power Supply	VDD, DACVDD, PLLVDD	-0.5	3.8	Volts
Signal Pin Voltage		-0.5	5.5	Volts
DAC Output Short Circuit Duration	T_{SC}		∞	seconds
Case Temperature	T_C	0	145	°C
Soldering Temperature (5 seconds, 0.25 in. from case)	T_{SOL}		260	°C
Vapor Phase Soldering Temperature (1 minute)	$T_{V,SOL}$		220	°C

Table 15. DC Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
DAC Outputs					
Resolution		8	8	8	Bits
Integral Linearity Error	ILE			3/4	LSB
Differential Linearity Error	DLE			3/4	LSB
Grey Scale Error				5	% Grey Scale
Monotonicity		Guaranteed	Guaranteed	Guaranteed	
Coding					Binary
CMOS Digital Inputs					
Input High Voltage (V_{DD} = 3.3 V)	V_{IH}	2.0		5.5	Volts
Input Low Voltage	V_{IL}	-0.5		0.8	Volts
Input High Current (V_{IH} = 2.4V)	I_{IH}			20	µA
Input Low Current (V_{IL} = 0.0V)	I_{IL}	-20			µA
Input Capacitance (f=1 MHz, V_{IN}=2.4V)	C_{IN}		4	8	pF
Digital Outputs (Except DIGICLK, DIGIBLK, DIGIRED, GRN, BLU)					
Output High Voltage (I_{OH} = -12 mA)	V_{OH}	2.4			Volts
Output Low Voltage (I_{OL} = 6 mA)	V_{OL}			0.4	Volts
Hi-Z Current ($0 \leq V \leq 3.6$ V)	I_{OZ}	-20		20	µA
Digital Outputs (DIGICLK, DIGIBLK, DIGIRED, GRN, BLU)					
Output High Voltage (I_{OH} = - 8 mA)	V_{OH}	2.4			Volts
Output Low Voltage (I_{OL} = 4 mA)	V_{OL}			0.4	Volts
Hi-Z Current ($0 \leq V \leq 3.6$ V)	I_{OZ}	-20		20	µA
Analog Outputs					
DAC Inaccuracy				7	%
DAC-to-DAC Mismatch				5	%
Output Compliance	V_{OC}	-0.5		1.2	Volts

Table 16. AC Characteristics

Parameter	Symbol	Spec.	170 MHz	220 MHz	250 MHz	Units
RS[2:0] Setup	t_1	min	10	10	10	ns
RS[2:0] Hold	t_2	min	10	10	10	ns
$\overline{RD}$, $\overline{WR}$ Low	t_3	min	50	50	50	ns
$\overline{RD}$, $\overline{WR}$ High	t_4	min	6 × pclk	6 × pclk	6 × pclk	ns
$\overline{RD}$ Low to Data Bus Driven	t_5	min	2	2	2	ns
$\overline{RD}$ Low to Data Bus Valid	t_6	max	40	40	40	ns
$\overline{RD}$ High to Data Bus 3-Stated	t_7	max	20	20	20	ns
Data Bus Hold from $\overline{RD}$ High	t_8	min	2	2	2	ns
Write Data Setup	t_9	min	10	10	10	ns
Write Data Hold	t_{10}	min	10	10	10	ns
LCLK, SCLK Low	t_{11}	min	4	4	4	ns
LCLK, SCLK High	t_{12}	min	4	4	4	ns
LCLK, SCLK Cycle	t_{13}					
16:1 MUX Mode		max	10.6	13.75	15.63	MHz
8:1 MUX Mode		max	21.25	27.5	31.25	MHz
4:1 MUX Mode		max	42.5	55	62.5	MHz
2:1 MUX Mode		max	85	100	100	MHz
1:1 MUX Mode		max	100	100	100	MHz
16:1 MUX Mode		min	94.12	72.7	64	ns
8:1 MUX Mode		min	47.06	36.4	32	ns
4:1 MUX Mode		min	23.53	18.2	16	ns
2:1 MUX Mode		min	11.77	10	10	ns
1:1 MUX Mode		min	10	10	10	ns
PIX[63:0] Setup	t_{14}	min	1	1	1	ns
PIX[63:0] Hold	t_{15}					
1:1 MUX Mode		min	4	4	4	ns
Not 1:1 MUX Mode		min	2	2	2	ns
VGA[7:0], $\overline{BLANK}$, $\overline{BORDER}/\overline{OE}$, $\overline{HCSYNCIN}$ Setup	t_{16}	min	3	3	3	ns
VGA[7:0], $\overline{BLANK}$, $\overline{BORDER}/\overline{OE}$, $\overline{HCSYNCIN}$ Hold	t_{17}	min	3	3	3	ns
SCLK to LCLK skew	t_{18}	min	-2	-2	-2	ns
(T=SCLK cycle time)		max	T-8	T-8	T-8	ns
DIGI CLK Cycle Time	t_{19}	min	18	18	18	ns
DIGI CLK Low (1)	t_{20}	min	t_{19} x 0.40	t_{19} x 0.40	t_{19} x 0.40	ns
		max	t_{19} x 0.60	t_{19} x 0.60	t_{19} x 0.60	ns
DIGI CLK High (1)	t_{21}	min	t_{19} x 0.40	t_{19} x 0.40	t_{19} x 0.40	ns
		max	t_{19} x 0.60	t_{19} x 0.60	t_{19} x 0.60	ns
Full Speed DIGI CLK: (2)						
DIGI BLANK setup	t_{22}	min	$t_{19}/2$ - 1.5	$t_{19}/2$ - 1.5	$t_{19}/2$ - 1.5	ns
DIGI BLANK hold	t_{23}	min	$t_{19}/2$ - 1.0	$t_{19}/2$ - 1.0	$t_{19}/2$ - 1.0	ns
DIGI DATA setup	t_{24}	min	$t_{19}/2$ - 4.0	$t_{19}/2$ - 4.0	$t_{19}/2$ - 4.0	ns
DIGI DATA hold	t_{25}	min	$t_{19}/2$ - 2.0	$t_{19}/2$ - 2.0	$t_{19}/2$ - 2.0	ns
Half Speed DIGI CLK: (2)						
DIGI BLANK setup	t_{22}	min	$t_{19}/4$ + 1.0	$t_{19}/4$ + 1.0	$t_{19}/4$ + 1.0	ns
DIGI BLANK hold	t_{23}	min	$t_{19}/4$ - 2.0	$t_{19}/4$ - 2.0	$t_{19}/4$ - 2.0	ns
DIGI DATA setup	t_{24}	min	$t_{19}/4$ - 2.5	$t_{19}/4$ - 2.5	$t_{19}/4$ - 2.5	ns
DIGI DATA hold	t_{25}	min	$t_{19}/4$ - 2.0	$t_{19}/4$ - 2.0	$t_{19}/4$ - 2.0	ns
Supply Current (3)		typ(4)	TBD	TBD	TBD	mA
		max(5)	TBD	TBD	TBD	mA

Notes:

1. DIGI CLK low/high times are for a 60/40 duty cycle.
2. Full Speed DIGI CLK is when Miscellaneous Control 4 register DIGI CDIV bit is set to 0; Half Speed DIGI CLK is when Miscellaneous Control 4 register DIGI CDIV bit is set to 1.
3. Supply current is the total of I_{VDD}, I_{VDDDAC} and I_{VDDPLL}.
4. Typical power dissipation is for VDD, VDDDAC, VDDPLL = 3.3 V, T_A = 20 °C, with typical pixel patterns such as displayed with graphical user interfaces, and
   170 MHz part running at 135 MHz (e.g., for 1280 x 1024 screen)
   220 MHz part running at 216 MHz (e.g., for 1600 x 1280 screen)
   250 MHz part running at 220 MHz
5. Maximum power dissipation is for VDD, VDDDAC, VDDPLL = 3.6 V, T_A = 0 °C, with alternating full black/full white pixels running at the maximum specified frequency (170/220/250 MHz)

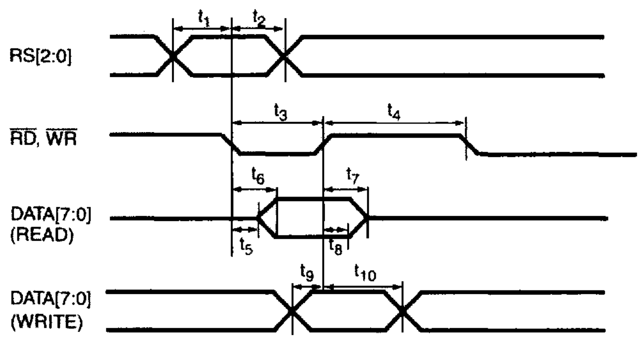


Figure 5. Microprocessor Interface Timing

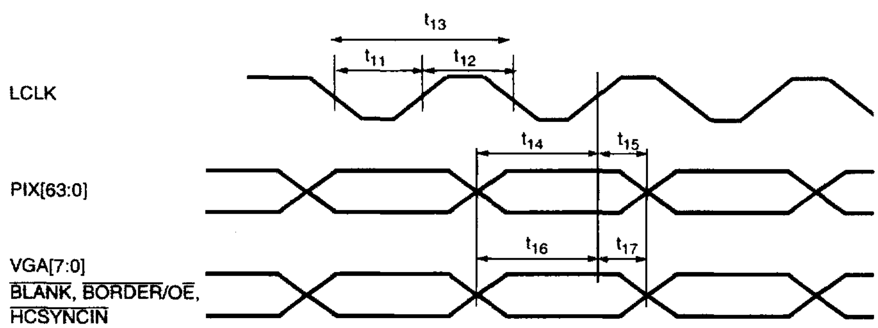


Figure 6. Pixel Data and Video Control Interface Timing

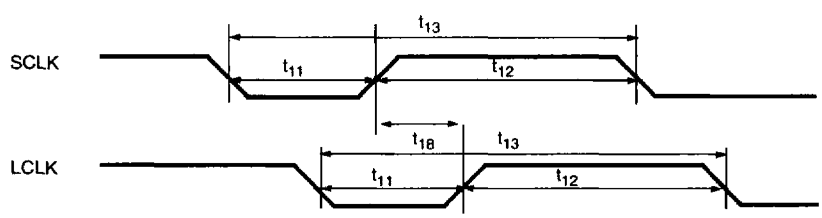


Figure 7. SCLK and LCLK Timing

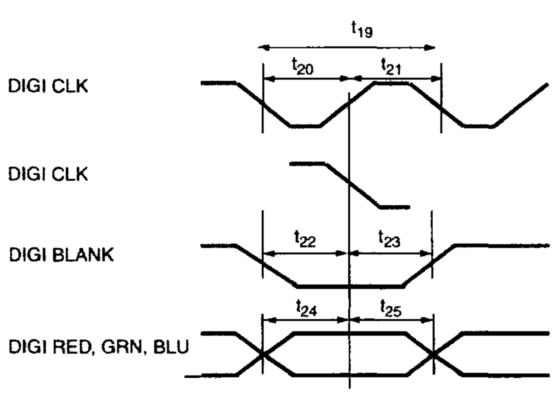


Figure 8. Digital Output Timings

14.0 Video Waveforms

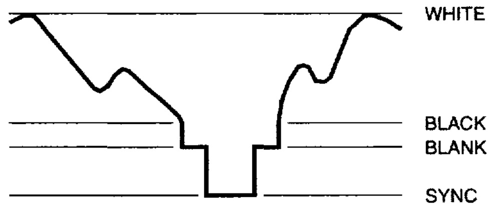


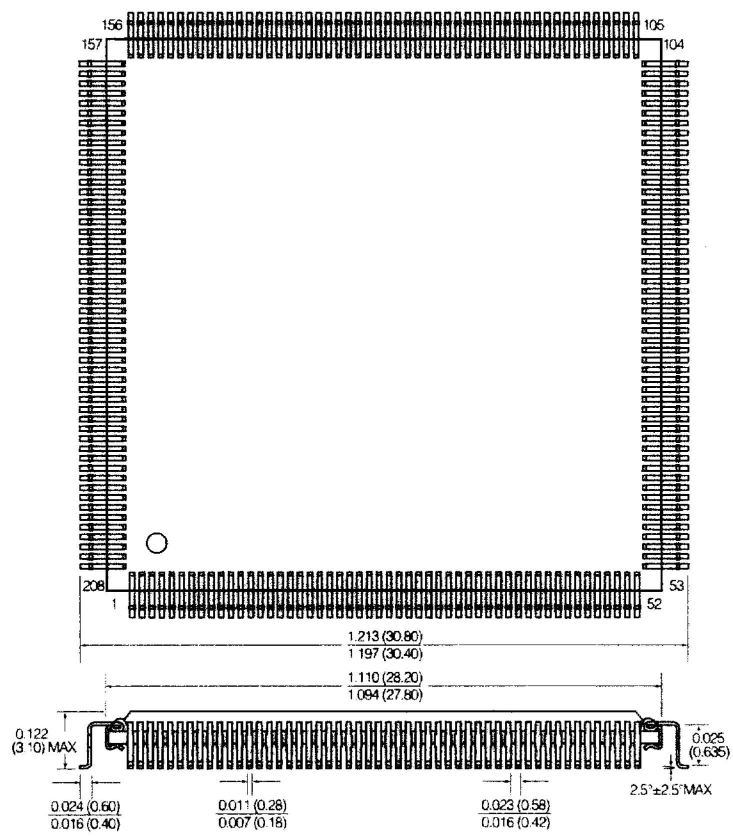
Table 17. Composite Video Output Waveform

	Doubly terminated 75 ohms, RREF=698 ohms											
Sync	**No**			**No**			**Yes**			**Yes**		
Pedestal	**No**			**Yes**			**No**			**Yes**		
Value	**IRE**	**mA**	**V**	**IRE**	**mA**	**V**	**IRE**	**mA**	**V**	**IRE**	**mA**	**V**
WHITE	100	18.65	0.70	92.5	19.05	0.714	100	26.67	1.00	92.5	26.67	1.00
BLACK		0	0	7.5	1.43	0.054		8.02	0.30	7.5	9.05	0.340
BLANK					0	0	-43				7.62	0.286
SYNC								0	0	-40	0	0
Note: RS-343A levels and tolerances assumed on all levels.												

Table 18. Composite Video Output Waveform

	Doubly terminated 100 ohms, RREF=927 ohms											
Sync	**No**			**No**			**Yes**			**Yes**		
Pedestal	**No**			**Yes**			**No**			**Yes**		
Value	**IRE**	**mA**	**V**	**IRE**	**mA**	**V**	**IRE**	**mA**	**V**	**IRE**	**mA**	**V**
WHITE	100	13.99	0.70	92.5	14.28	0.714	100	20.00	1.00	92.5	20.00	1.00
BLACK		0	0	7.5	1.07	0.054		6.01	0.30	7.5	6.78	0.340
BLANK					0	0	-43				5.71	0.286
SYNC								0	0	-40	0	0
Note: RS-343A levels and tolerances assumed on all levels.												

15.0 Package Information



16.0 Ordering Information

Table 19. Part Numbers

Part Number	Speed
IBM 37RGB528 CF 17-A	170 MHz
IBM 37RGB528 CF 22-A	220 MHz
IBM 37RGB528 CF 25-A	250 MHz

17.0 Change Summary

Table 20. Summary of Changes

Date	Changes
05/09/94	1. First publication.
07/20/94	1. Corrected description of pixel PLL operation following a reset. Section 2.7.1, "Pixel PLL," now indicates that the PLL will run at a frequency in the kilohertz range following a reset (or when it is "disabled"). The values of the PLL Control 2 register, and the PLL programming registers F0 - F15 are now shown to have reset values of 0x00. These values will cause the pixel frequency to be in the range of 1.25 KHz to 62.5 KHz following a reset. Also indicated that SYSCLK PLL will run in kilohertz range when disabled. The SYSCLK PLL operation following a reset continues to be the same: it comes up enabled at a pre-programmed frequency. 2. In section 2.8, "PLL Programming," a statement was removed that indicated a check for minimum VRF was unnecessary for M over N programming with an input reference above 4 MHz. This is not true. 3. Table 11, "Pin Descriptions," on page 59, $\overline{\text{VGAMODE}}$ changed to VGAMODE, $\overline{\text{TESTMODE}}$ changed to TESTMODE. 4. Table 12, "Signal List by Pin Number," on page 66, PX[89]/DBLK changed to PX[89]/DBLK (pin 200). 5. "Miscellaneous Control 1," on page 36, bit 6, VMSK CNTL, changed PIX[63:0] to PIX[127:0]; and corresponding text was changed from "The VRAM inputs on the PIX[63:00] inputs will be masked under control of the VRAM Mask High and VRAM Mask Low registers" to read "The VRAM inputs on the PIX[127:00] inputs will be masked under control of the VRAM Mask 0, 1, 2, and 3 registers." 6. 4.5, "Sync Control," on page 20, changed PIX[63:0] to PIX[127:0]. 7. Section 3.4.4, "24 BPP," and "Pixel Format Register" description redefined stating that if 24 BPP Packed format is selected with the Pixel Format register, but the VRAM SIZE bits in the Miscellaneous Control 1 register are set for 32 bits, then the product operation is undefined. 8. Table 16, "AC Characteristics," on page 68, refined DIGI BLANK and DIGI DATA setup and hold times. 9. 11.2.7, "Diagnostic Support," the Power on Value for the ID register is changed from 0x01 to 0x02. 10. Fixed incorrect cross references. 11. Cross references expanded to include section numbers with headings where applicable. 12. Expanded the table of contents to include register description headings and page numbers. 13. Miscellaneous typographical errors corrected.

Table 20. Summary of Changes (Continued)

Date	Changes
06/26/95	The following changes supplement or correct the 07/20/94 revision and apply to all versions of the RGB528: 1. Corrected typos in Table 2, "SCLK Frequencies," on page 5. For VRAM=128, the SCLK divide factor was incorrect for BPP of 4, 8, 15/16, and 32. 2. Added a note to section 2.5.1, "DDOTCLK," that there is no particular phase relationship between DDOTCLK and SCLK. 3. Added section 2.13, "PLL Interaction," describing a programming requirement to prevent the two PLLs from interfering with each other. 4. Changed 8.4, "PLL Power," to indicate that each PLL can be individually disabled. Also removed a statement that the PLLs draw 3 mW of power, and added a statement that the PLLs draw standby current when disabled. 5. Added note to Section 10.0, "Internal Register - Summary," requiring setting of reserved register bits to '0', and not writing to reserved registers. 6. Deleted the value found in the Revision Level register (page page 56.) This value is specific to the product revision level, and is now given in Appendix C.0, "-A Revision Level". 7. Fixed typo in Table 11. The bit range for the Digital Outputs is PIX[89:64], not PIX[89:63]. 8. Fixed typo in Table 17 and Table 18. For Sync = Yes and Pedestal = No, the IRE value for the sync tip is changed from -30 units to -43 units, for both tables. 9. Added appendix B.0 , "Switching Into VGA Mode," on page 76. This appendix recommends a particular software sequence for switching from the VRAM port to the VGA port, for compatibility with the RGB513, RGB514, and RGB525 products. The remaining changes are specific to the "-A" product revision (RGB528A): 10. Changed name everywhere from RGB528 to RGB528A. 11. Updated Figure 1 on page 5 to show new SCLK width for a 16/3 CLK. When the pixel format is "24 Packed", and the VRAM width is 128, the 16/3 clock produced for SCLK has an "up" time of 2 PCLK periods. 12. Changed 6.3, "DSR - DAC Slew Rate," to indicate that the DSR bit in the DAC Operation register is disabled. The DACs are permanently set to the "fast" slew rate setting. Made the same change to the description of the DAC Operation register on page page 42. 13. Changed 8.1, "DAC Power," to indicate that a standby current is drawn when the DACs are disabled with the DAC PWR bit. 14. Changed part numbers for ordering In Table 19 (e.g. from "IBM37-RGB528-CF-17C" to "IBM 37RGB528 CF 17-A"). 15. Added Appendix C.0, "-A Revision Level".
05/29/97	1. In Table 13, "Recommended Operating Conditions," on page 67, changed the power supply voltage specification to 3.6V ± 0.5% for the 250 MHz part only. 2. Removed "Preliminary" designation.

Appendix

A.0 Relationship to RGB525

The RGB528A is a superset of the RGB525 and is generally upward register compatible with the RGB525. The RGB528A adds these features:

- A second programmable clock generator is added for driving SYSCLK. This clock is also known as MCLK.
- The VRAM pixel input is expanded from 64 bits to 128 bits.
- Two dual buffer modes are added:
  1. Dual 64-bit buffer - using the 128-bit VRAM interface, either the low 64 bits or the high 64 bits are chosen for the pixel data, under register control. Within the chosen 64 bits any format may be used (4,8,16,24,32 BPP).
  2. 8 BPP - the incoming pixel data is treated as pairs of 8 bit pixels, with one or the other chosen under register control. The only format is 8 BPP, but any VRAM width may be used.
- The internal pixel data just prior to the DACs, is brought out as digital outputs for driving flat panel displays.

In addition, there are these functional differences:

1. The VGA inputs are shared with the high 8 bits of the 128-bit VRAM pixel inputs. To aid in 3-stating these signals at the card level, the signal VGAMODE is brought out. This is the inverted state of the PORTSEL bit in the Miscellaneous Control 2 register.
2. The $\overline{\text{HCSYNCIN}}$ input on the RGB528A is two separate inputs on the RGB525: $\overline{\text{HSYNCIN}}$ and $\overline{\text{CSYNCIN}}$.
3. The $\overline{\text{BORDER}}$/$\overline{\text{OE}}$ input on the RGB528A is two separate inputs on the RGB525: BORDER and ODD/$\overline{\text{EVEN}}$. A new bit, BRDR/INTL, is added to the Miscellaneous Control 2 register to select the function of this input.
4. The RGB525 has an input, "EXTCLK", which can serve as an alternate to the REFCLK input, either as the input reference to the PLL, or as the pixel clock. The RGB528A does not have this input.

   On the RGB525 bit 4 of the PLL Control 1 register selects the reference source of the PLL, REFCLK or EXTCLK. On the RGB528A this bit is reserved.

   Bits 7 - 6 of the Miscellaneous Control 2 register select the source of the pixel clock. On the RGB525 a setting of '10' will select EXTCLK. On the RGB528A this setting selects REFCLK.
5. The RGB525 pixel clock generator resets to the "off" condition and must be programmed before it is enabled. This allows a wide range of incoming REFCLK frequencies.

   The RGB528A pixel clock generator is the same, but the new SYSCLK PLL powers up enabled, with default programming values. REFCLK is shared between the two PLLs. This may restrict the REFCLK frequency, depending on how the generated SYSCLK is used at reset time.
6. System Clock Control (index 0x0008), System PLL Reference Divider (index 0x0015), and System PLL VCO Divider (index 0x0016) registers are added for controlling and programming the SYSCLK PLL.
7. The Miscellaneous Clock Control register has a bit added, SCLK INVT, that inverts the out-going SCLK. This is intended as an aid for meeting tight timings at the card level.
8. Two external frequency selects FS[3], FS[2] are eliminated. This restricts the external pixel frequency selection to four sets of values. Using internal selection, 16 values (direct programming) or 8 values (M/N programming) can still be chosen, the same as for the RGB525.
9. The ID register is changed to a value of "0x02".
10. The Miscellaneous Control 1 register now has two bits to represent the VRAM size, to accommodate the new width of 128.
11. In the Miscellaneous Control 3 register, the SWAP WORD bit is deleted. SWAP DWRD is added, to swap between the low and high 64 bits with a VRAM width of 128.
12. Miscellaneous Control 4 register (index 0x0073) is added to control the dual buffer modes and set the operation of the Digital Output interface. Buffer A/B Select register (index 000f) is added to control selection of the A or B buffer in the dual buffer modes.
13. To accommodate the 128-bit VRAM interface, two additional VRAM Mask registers are added, and the four Mask registers are now labeled 1, 2, 3, 4

(Indices 0x0090, 0x0091, 0x0092, 0x0093).

14. The RGB525 pixel PLL requires two external resistors RPLLI and REXT. The two PLLs on the RGB528A do not require these resistors. Each PLL still requires external loop filter components.
15. The RGB525 $\overline{\text{TESTMODE}}$ input is TESTMODE on the RGB528A. TESTMODE now has an internal pull-down resistor, so it may be left unconnected at the card level.

B.0 Switching Into VGA Mode

The RGB528A has two fundamental modes of operation which depend on the input pixel port selected, VGA or VRAM. The port is selected with the "PORT SEL" bit (bit 0) of Miscellaneous Control 2 register.

On the RGB513, RGB514, and RGB525 products, there are two problems that can occur when switching from the VRAM port back to the VGA port. Internally latched data from the previously selected VRAM port can corrupt the VGA data, and the SCLK can stop running momentarily. Both of these problems can be circumvented with a software work-around.

For software compatibility with the RGB513, RGB514, and RGB525 it is recommended that this software work-around also be incorporated in the software used with the RGB528A. The RGB528A does not require this software modification, but it does continue to operate correctly (that is, the software patch is transparent to the RGB528A.)

The software modification is as follows:

When doing a "mode switch" into VGA mode, the following additional steps should be taken:

1. Set bits 1 and 0 to '1's in VRAM Mask Low register, to mask off the lowest VRAM byte. The remaining VRAM Mask bits are "don't care".
2. Set bit 6 (VMSK CNTL) in Miscellaneous Control 1 register to '1', to enable the VRAM MASKing.
3. Make sure at least one SCLK occurs. This means setting up the chip for VRAM pixel data operation. In particular, make sure that the Pixel Format register is set to one of the valid formats (4 BPP...32 BPP). A valid pixel format must be set or SCLK will not run.
4. At this point the low byte of the internal VRAM pixel data should be '0's, and will not interfere with the VGA data.

The VGA Port can now be selected. A two step process is required:

1. Write to the Miscellaneous Control 2 register. Set bit 0 (PORT SEL) to '0' for VGA, but write bits 7 and 6 as '01' (PCLK SEL = Internal PLL.)
2. Do a second write to the Miscellaneous Control 2 register. Again, set bit 0 (PORT SEL) to '0' for VGA. But now set bits 7 and 6 to '00' (PCLK SEL = LCLK.) The VGA port is now selected.

When doing a mode switch back to VRAM port operation, make sure that bit 6 (VMSK CNTL) in Miscellaneous Control 1 register is set back to '0', to disable the VRAM MASKing.

C.0 -A Revision Level

The original RGB528 is replaced with the "-A" revision (RGB528A). The new revision has the following changes from the original:

1. The RGB528A has a bit in the Miscellaneous Clock Control register (index 0x0002) called SCLK INVT. This bit, when set, inverts the signal on the SCLK output pin. The purpose of this function is to change the timing relationship between the outgoing SCLK and the incoming LCLK. This can help guarantee an AC timing specification in Table 16 called "SCLK to LCLK skew" (symbol t_{18}.)

   On the original RGB528 this function can appear to be working correctly, but internally there is a problem that can cause the incoming pixel data and control signals to be latched incorrectly. The RGB528A fixes this problem.

2. The SCLK output is generally a symmetric clock that is a "divide down" of the internal pixel clock. For the "24 packed" pixel format, in which an odd number of SCLKs is generated from an even number of pixel clocks, by necessity the SCLK output is asymmetric.

   On the original RGB528 for 24 packed pixel format, with a VRAM width of 128 bits, the generated SCLK has a relatively short up time compared to the down time. On the RGB528A the up time is lengthened. While still asymmetric, the up and down times are more closely matched as compared to the original device. (Figure 1 on page 5.)

   The intent of this change is to make it easier at the board level to guarantee the VRAM serial clock up level time.

3. The performance of the three DAC outputs, red, green and blue, is improved slightly.

   The DACs are clocked by the internal pixel clock, and only change value on pixel clock boundaries. There is a slight delay internally from the pixel clock edge to the output of the DAC.

   On the original RGB528, there is slightly more delay for positive going outputs than negative going outputs. For large transitions (such as a single pixel that goes from black to full intensity and back to black), this can cause a slight narrowing of the output pulse.

   The RGB528A removes some internal delay in the DACs and makes the slew rates slightly faster.

4. The DAC Operation register (index 0x0006) has a bit DSR (bit 1) for controlling the DAC Slew Rate (slow or fast). On the RGB528A this bit has no function. It can be written and read, but the DAC outputs will always have a "fast" slew rate.

   This change is a consequence of changing the DAC slew performance, as described above.

5. The Power Management register (index 0x0005) has a bit DAC PWR (bit 0) for turning off power to the analog portion of the DACs. Although not specified in the data sheet, on the original RGB528 the current drawn by the DACs is less than 1 mA (3.6 mW at 3.6 V) when the DAC PWR bit is set. (Note that this is just the internal DAC analog circuitry, not the entire Palette DAC.)

   On the RGB528A when the DAC PWR bit is set the current drawn by the internal DAC circuits is less than 20 mA (72 mW at 3.6 V.) The higher current draw (20 mA versus 1 mA) is a consequence of changing the DAC slew performance, as described above.

6. The contents of the Revision register (index 0x0000) changes from 0xf0 to 0xe0.