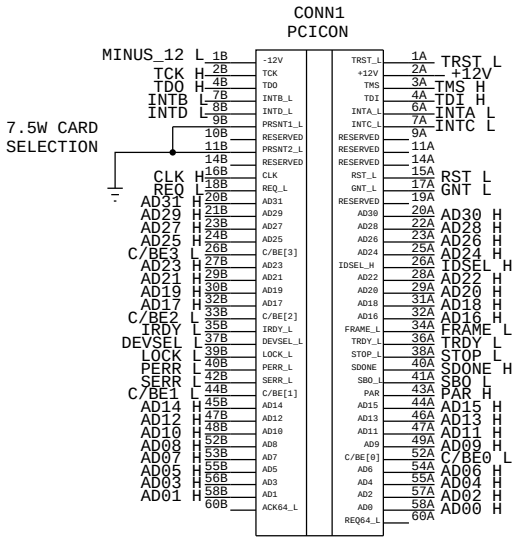
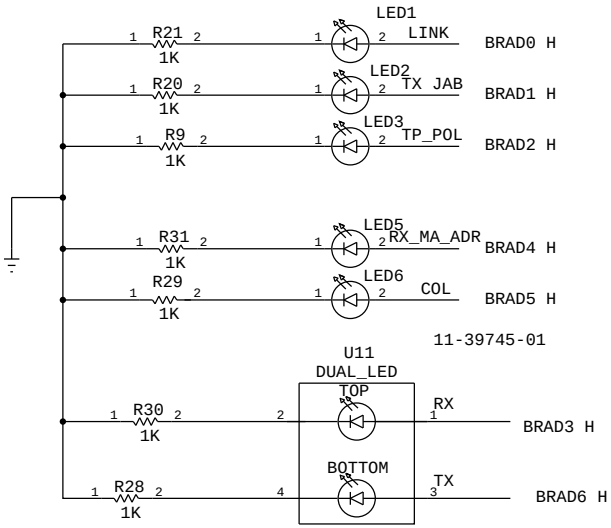
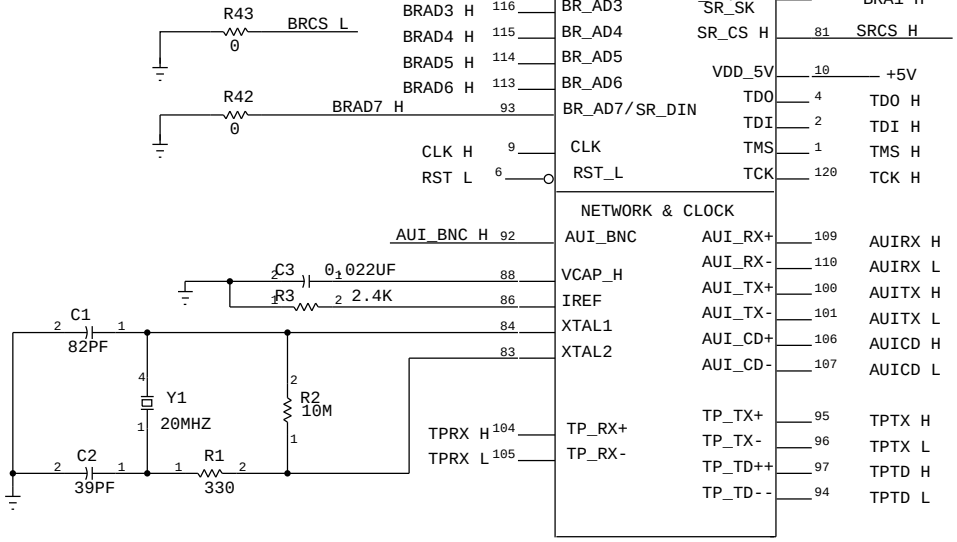
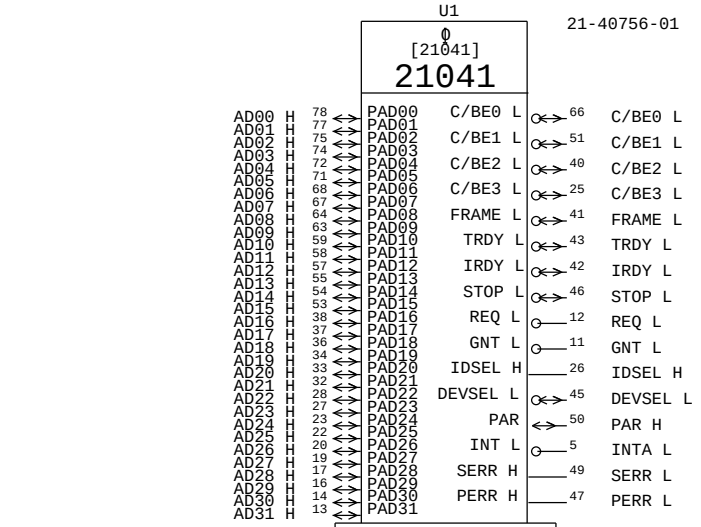
PCI CONNECTOR









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REVISION		
CHK	CHANGE NO.	REV
PTUB3		

DRAWING PTUB3 ...1

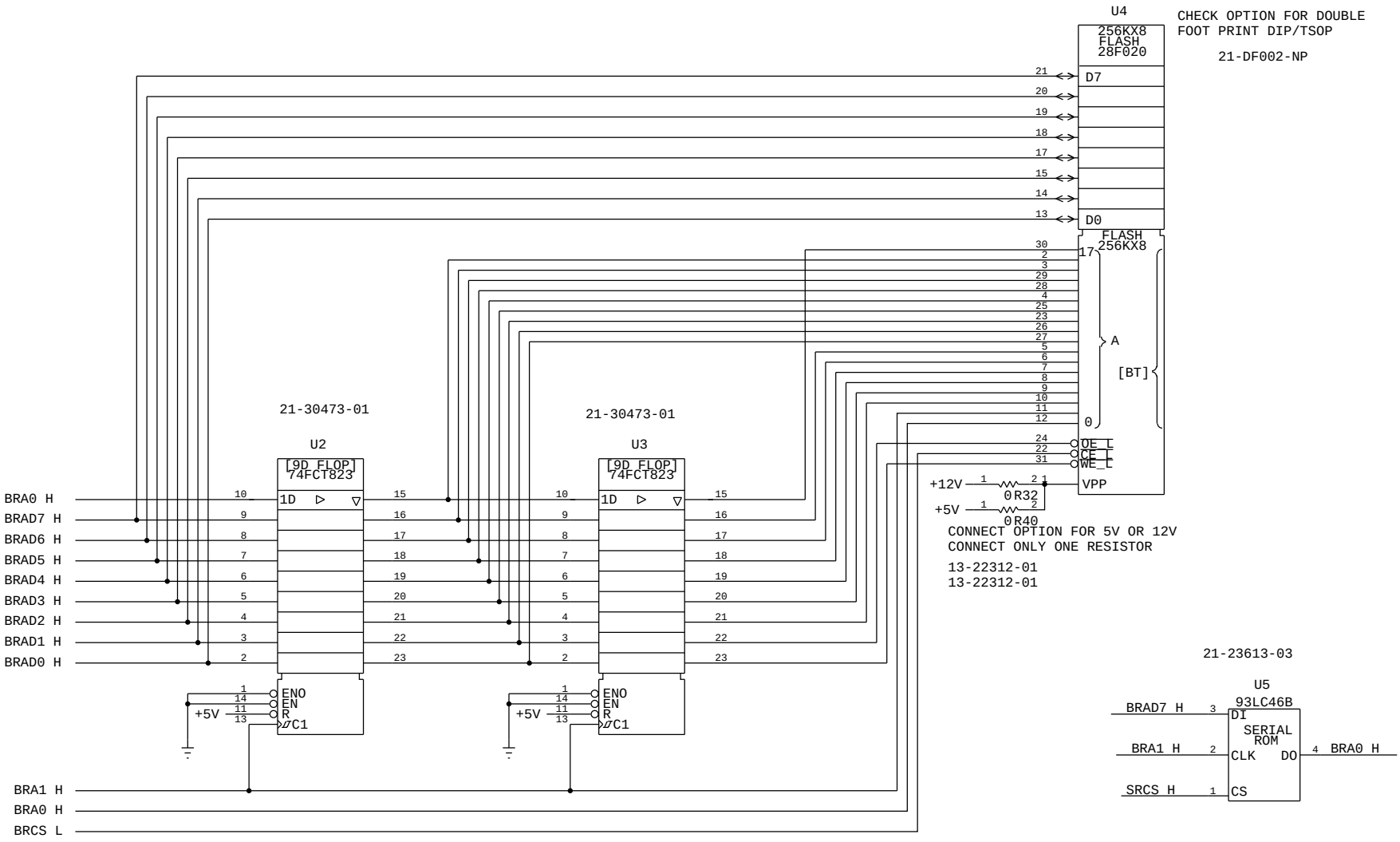
LAST_MODIFIED=Sun Apr 2 14:39:36 1995

digital

DRN.	DATE	ENG. YUVAL BACHAR	DATE
CHK'D.	DATE	BOARD LOCATION:	
USRA:		SHEET 1 OF 6	
FIRST USED ON OPTION/MODEL:		TOP DOCUMENT NUMBER: EC-QHUYA-TE	

TITLE: TULIP3

SIZE	CODE	NUMBER	REV.
B		54-24124-01	



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REVISION		
CHK	CHANGE NO.	REV
PTUB3		

DRAWING PTUB3 ...2

LAST_MODIFIED=Sun Apr 2 14:39:59 1995

digital

DRN. DATE
CHK'D. DATE
USRA:
FIRST USED ON OPTION/MODEL:

ENG YUVAL BACHAR DATE
BOARD LOCATION:
SHEET 2 OF 6
TOP DOCUMENT NUMBER: EC-QHUYA-TE

TITLE: BOOT & SER ROMS

SIZE	CODE	NUMBER	REV.
B		54-24124-01	

13-22312-01
13-22312-01
13-22312-01
13-22312-01

DON'T ASSEMBLY IF THE 244 IS ASSEMBLED
L.O. UNDER THE PACKAGE

0 R35
0 R37
0 R39
0 R34

U6
[OCTAL]
[DRIVER]
74ACT244

TPTX H
TPTD H
TPTX L
TPTD L
EN

19-26876-01

NOTE
IF THE 74ACT244 IS BYPASSED
USE THE FOLLOWING VALUES:
R4,R6=20 R5,R7=140 R8=510

R4 61.9
R5 301
R6 61.9
R7 301

R8
806 13-23828-88

TR1
TP FILTERS & BALUNS
78Z041

XMT
LPF

RCV
LPF

1:1
1:1

13-23827-77
13-23828-47
13-23827-77
13-23828-47

C4
0.1UF
C37
0.1UF

TPRX H
TPRX L

10-24053-09
10-24053-09
13-23827-68
13-23827-68

R33
50
R41
50

C74
0.1UF
10-24053-09

12-33220-01
U10
SHIELDED
RJ45
JACK

TD+
TD-
RD+
RD-
SHIELD
MP1
MP2

CHASIS L

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REVISION		
CHK	CHANGE NO.	REV
PTUB3		

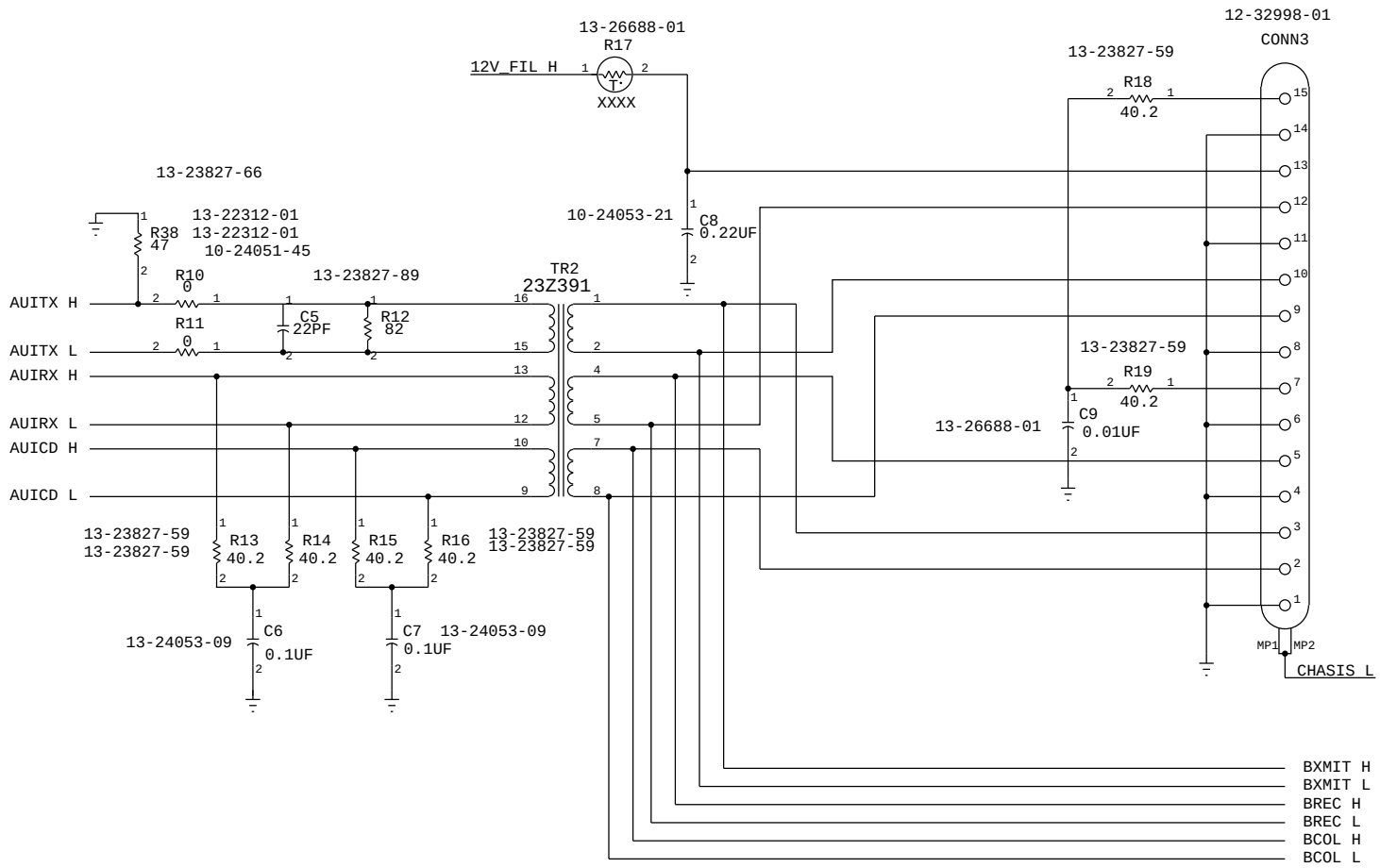
DRAWING PTUB3 ...3
LAST_MODIFIED=Sun Apr 2 14:45:07 1995

digital

DRN. DATE
CHK'D. DATE
USRA:
FIRST USED ON OPTION/MODEL:

ENG YUVAL BACHAR DATE
BOARD LOCATION:
SHEET 3 OF 6
TOP DOCUMENT NUMBER: EC-QHUYA-TE

TITLE: TP INTF
SIZE B | CODE | NUMBER 54-24124-01 | REV.



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REVISION		
CHK	CHANGE NO.	REV
PTUB3		

DRAWING PTUB3 ...4

LAST_MODIFIED=Sun Apr 2 14:48:59 1995

digital

DRN. DATE

CHK'D. DATE

USRA:

FIRST USED ON OPTION/MODEL:

ENG YUVAL BACHAR DATE

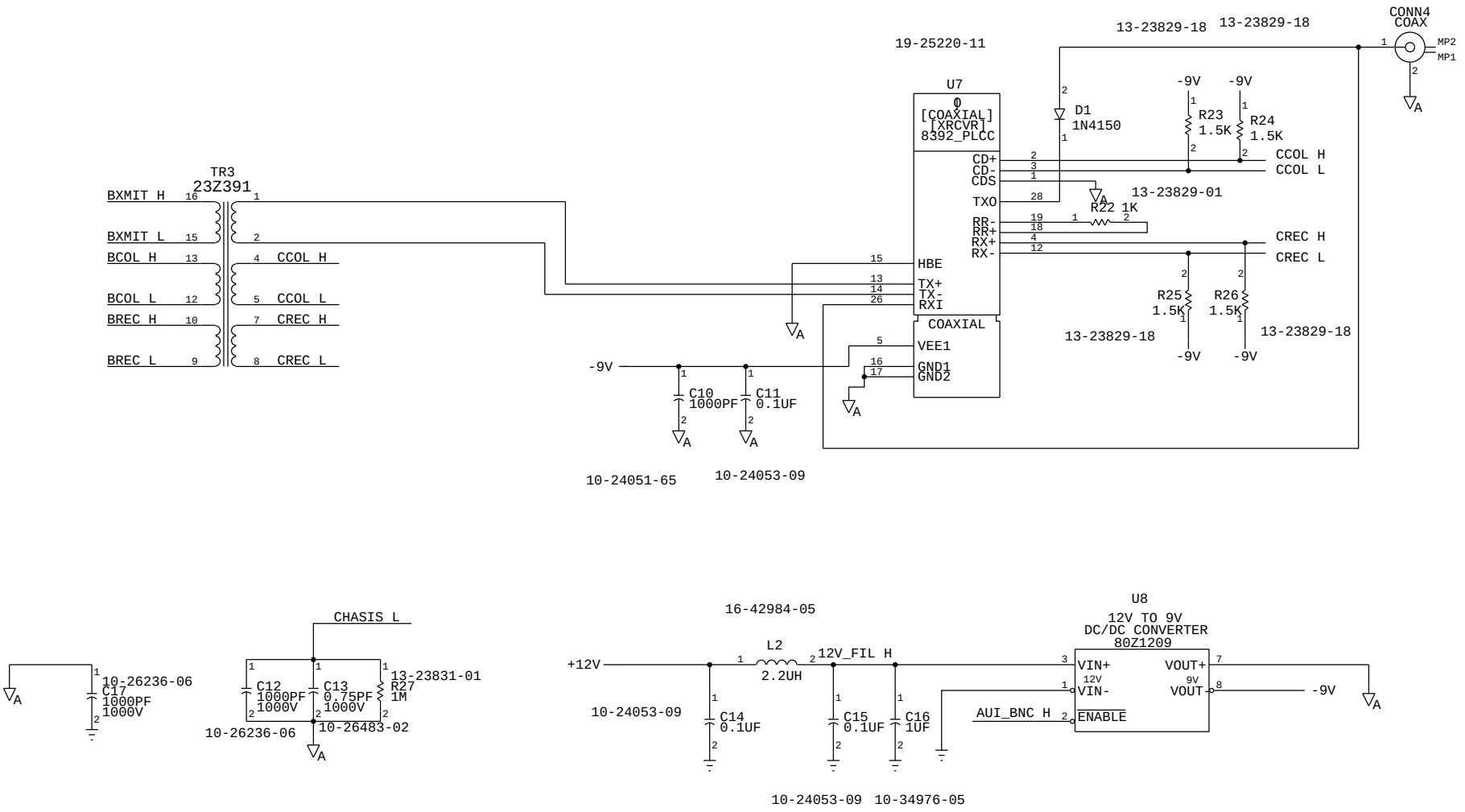
BOARD LOCATION:

SHEET 4 OF 6

TOP DOCUMENT NUMBER: EC-QHUYA-TE

TITLE: 10BASE5 INTF

SIZE	CODE	NUMBER	REV.
B		54-24124-01	



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REVISION		
CHK	CHANGE NO.	REV
PTUB3		

DRAWING PTUB3 ...5

LAST_MODIFIED=Sun Apr 2 14:49:43 1995

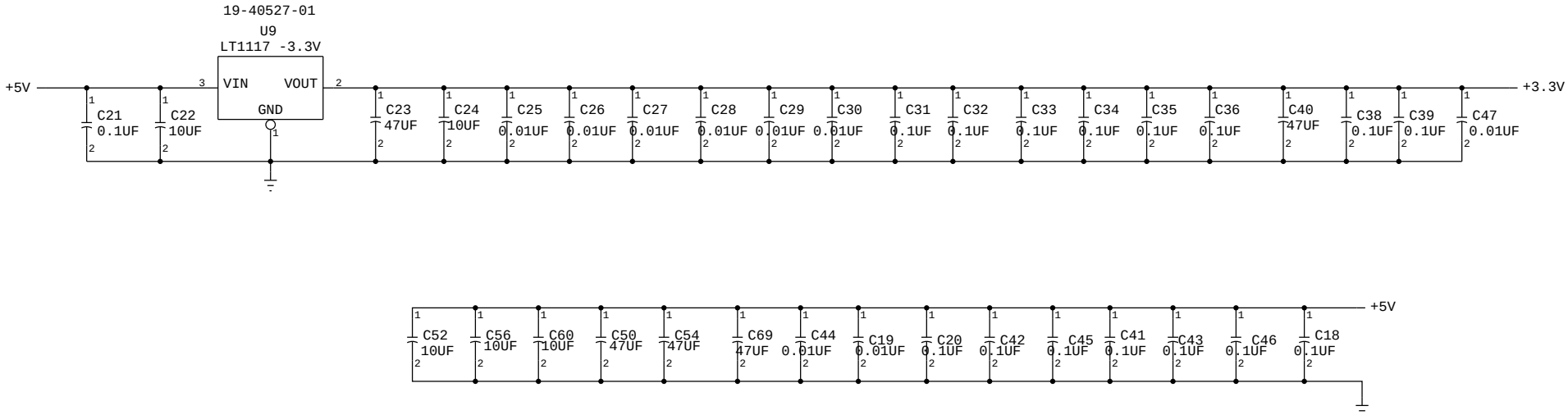
digital

DRN. DATE
CHK'D. DATE
USRA:
FIRST USED ON OPTION/MODEL:

ENG YUVAL BACHAR DATE
BOARD LOCATION:
SHEET 5 OF 6
TOP DOCUMENT NUMBER: EC-QHUYA-TE

TITLE: 10BASE2 INTF

SIZE	CODE	NUMBER	REV.
B		54-24124-01	



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REVISION		
CHK	CHANGE NO.	REV
PTUB3		

DRAWING PTUB3 ...6

LAST_MODIFIED=Sun Apr 2 14:50:03 1995

digital

DRN. DATE

CHK'D. DATE

USRA:

FIRST USED ON OPTION/MODEL:

ENG YUVAL BACHAR DATE

BOARD LOCATION:

SHEET 6 OF 6

TOP DOCUMENT NUMBER: EC-QHUYA-TE

TITLE: POWER SUPPLY

SIZE	CODE	NUMBER	REV.
B		54-24124-01	

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DATE	RESPONSIBLE ENGINEER	ECO NUMBER	REV

PRINTED WIRE BOARD LAYER CONSTRUCTION

LAYER	DIELECTRIC SPACING	LAYER TYPE	COPPER WEIGHT	LINE WIDTH(S)
1		SIGNAL	0.5 oz.+PLATING	.006
	0.009 +/- 0.0026			
2		PLANE	1.0 oz.	
	0.035 REFERENCE			
3		PLANE	1.0 oz.	
	0.009 +/- 0.0026			
4		SIGNAL	0.5 oz.+PLATING	.006

OVERALL THICKNESS SPECIFICATION=0.062 +/- 0.007 (PLATING-TO-PLATING)

1.0 oz. COPPER FOIL THICKNESS NOMINAL: .0014 (.0010 MIN. AFTER PROCESSING)

0.5 oz. COPPER FOIL THICKNESS NOMINAL: .0007 (.0003 MIN. AFTER PROCESSING)

OUTER LAYERS ARE STARTED WITH 0.5 oz. COPPER AND PLATED TO 0.0014 MINIMUM COPPER THICKNESS.

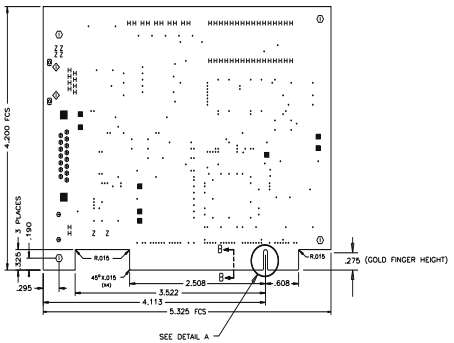
SIGNAL LINE WIDTH TOLERANCE = 0.006 +/- 0.0015

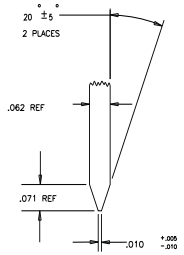
MINIMUM COPPER REQUIREMENT FOR PLATED THRU HOLE WALLS IS 0.0008

NOTES:

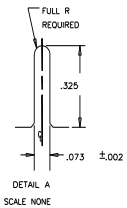
1. IF A CONFLICT BETWEEN THIS DOCUMENTATION/DESIGN PACKAGE AND ANY OTHER REFERENCED DOCUMENT EXISTS, THIS DOCUMENTATION/DESIGN PACKAGE WILL TAKE PRECEDENCE.
2. ALL ARTWORK FEATURES (IN ALL FORMATS) ARE SUPPLIED AT NOMINAL DIMENSIONS. UNLESS OTHERWISE SPECIFIED, THE FINISHED CIRCUIT SHOULD REFLECT THESE DIMENSIONS INCLUDING ALLOWABLE FABRICATION TOLERANCES PER DIGITAL STANDARD 176. ALL ARTWORK AND DRILL FEATURES MAY BE MODIFIED TO ACCOMMODATE SPECIFIC FABRICATION PROCESSES.
3. DIELECTRIC MATERIAL TO BE FR4 WITH A MINIMUM GLASS TRANSITION TEMPERATURE OF 125 C. °
4. ALL COPPER FOIL SHALL MEET OR EXCEED ANSI/IPC CF-150 TYPE ED (ELECTRODEPOSITED) CLASS 1 REQUIREMENTS.
5. LIQUID PHOTOIMAGABLE SOLDERMASK (LPISM) IS REQUIRED ON BOTH SIDES OF THE PWB. NO SOLDERMASK WILL BE PERMITTED ON THE TOP (SOLDERABLE SURFACE) OF ANY SURFACE MOUNT DEVICE PADS.
6. NICKEL AND GOLD PLATE FINGER SET AREA PER DIGITAL STANDARD 176. VENDOR TO ADD PLATING BUSS BAR FOR EACH CIRCUIT.
7. ALL .015"(.38mm) DIAMETER HOLES ARE TO BE DRILLED .015"(.38mm) MINIMUM DIAMETER.

* NOTES CONTINUED ON SHEET 2 *





SECTION B-B
2 PLACES
SCALE NONE



DETAIL A
SCALE NONE

HOLE DATA (FOR STANDARD HOLE TOLERANCES USE DEC STD 176)												
SYMBOL	•	■	H	⊕	Z	■	@	⊕	■	①	◇	
FINISHED HOLE SIZE (INCHES)	.015	.030	.038	.040	.042	.047	.062	.083	.130	.125	.128	
POSITIVE TOLERANCE (INCHES)	.003											
NEGATIVE TOLERANCE (INCHES)	.015											
FINISHED HOLE SIZE (mm)												
POSITIVE TOLERANCE (mm)												
NEGATIVE TOLERANCE (mm)												
PLATED	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	
QUANTITY	227	6	52	15	6	2	2	2	2	4	2	

FROM LAYER 1 TO LAYER 4

FABRICATION INFORMATION: MATERIAL AND WORKMANSHIP FOR ALL FABRICATED PRINTED WIRING BOARDS MUST MEET THE REQUIREMENTS OF DEC STD 176

FABRICATE BOARD PER: SEE SHEET 2 AS SHOWN ____ | STEP AND REPEAT CODE: 2CB235 | PRESS FIT COMPONENTS: YES ____ NO X

DESIGN INFORMATION	
NUMBER OF LAYERS: 4	LAYER CONSTRUCTION: AS SHOWN X
CONTROLLED IMPEDANCE: YES ____ NO X	CONTROLLED CAPACITANCE: YES ____ NO X
SURFACE MOUNT TECH / MINIMUM PITCH:	SIDE 1 .80MM SIDE 2 >.050
PLANAR RESISTOR TECHNOLOGY: YES ____ NO X	NUMBER OF PRT LAYERS ____
BOARD FINISH: REFLOW TIN LEAD X	HASL ____ ALL COPPER ____ OTHER ____
SOLDERMASK: NONE ____ SIDE 1 X	SIDE 2 X SMOBC: YES ____ NO X
NOMENCLATURE: NONE ____ SIDE 1 X	SIDE 2 X TENTED VIAS: YES ____ NO X
MINIMUM VIA HOLE SIZE: .015	MINIMUM COMPONENT HOLE SIZE: .038
PAD EXPANSION: OUTER LAYERS X	SIGNAL INNER LAYERS ____ NONE ____
INCIRCUIT THIEVING: NONE ____ SIDE 1 X	SIDE 2 X AS SHOWN ____
TECHNOLOGY (LW/LS): LINE .006	SPACE .007
CIRCUIT OUTLINE/FINGER DETAIL:	AS SHOWN X
SPECIAL REQUIREMENTS:	

TOLERANCES				
INCHES UNLESS OTHERWISE SPECIFIED		mm		ANGLES
.XXX ± .010	.XX ± .25			±0 DEG
.XX ± .020	.X ± .50			30 MIN
.X ± .100	X. ± 2.50			

APPROVALS	DATE
DRAWN: WHC	29 NOV 1994
CHECKED:	
MECH ENG:	
PROJ ENG:	
MFG ENG:	
SCALE: 1:1	
SHEET 1 OF 2	
TOP DOC NO: K-DD-5024124-0-0	

digital™

TITLE:

CIRCUIT DRILL AND ETCH DRAWING

SIZE	CODE	NUMBER	REV
D	MD	5024124-0-0	AX00
ETCH REV: A01			MEDIA X

WO#

5024124-0-0 AX00

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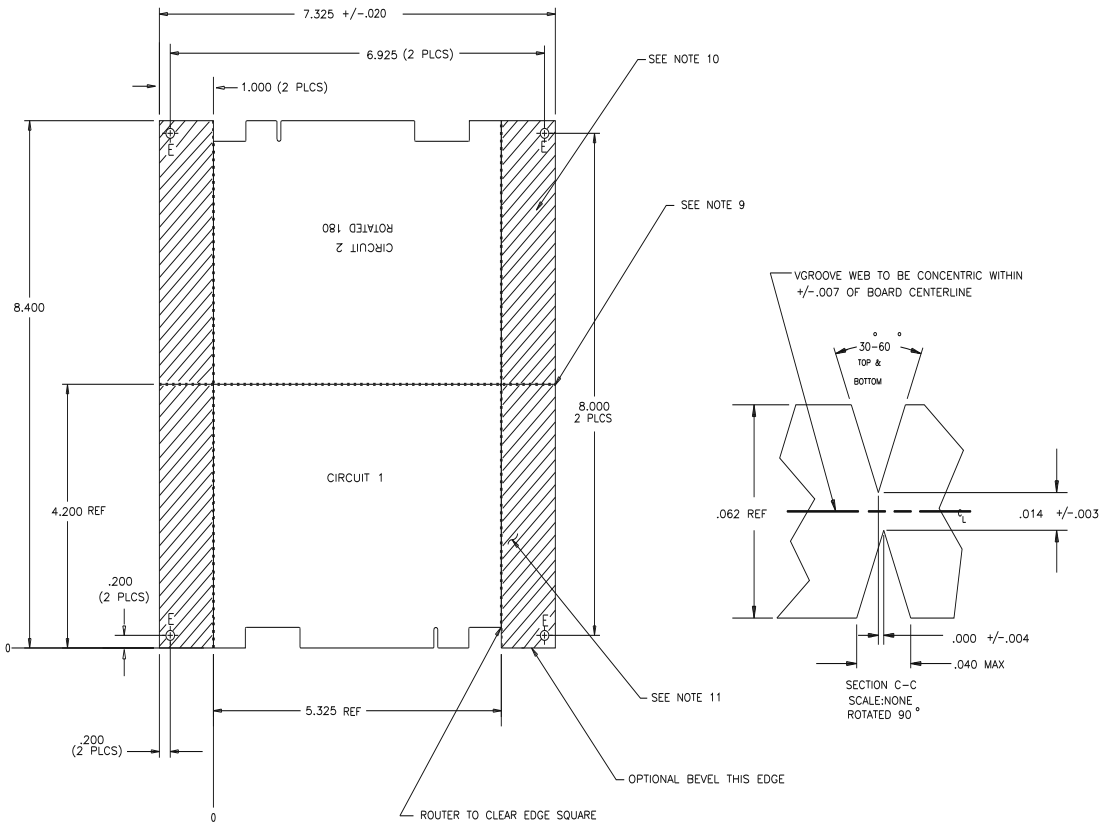
NOTES CONTINUED FROM SHEET 1;

9. EACH CIRCUIT TO BE V-GROOVED AS INDICATED BY DASHED LINES, THREE (3) PLACES. REFER TO SECTION C-C FOR ADDITIONAL INFORMATION.
10. AREAS INDICATED BY CROSSHATCH ARE TO REMAIN ON THE PWB FOR THE MANUFACTURING ASSEMBLY PROCESS. THE PWB FABRICATOR SHALL COVER ALL CROSSHATCHED AREAS WITH SOLDERMASK ON BOTH SIDES OF THE PWB. THE PWB FABRICATOR MAY UTILIZE ALL CROSSHATCHED AREAS AS PART OF THEIR PWB PROCESS PANEL TOOLING AREA. PWB PROCESS FABRICATION FEATURES (IE: TOOLING HOLES, TEST/DRILL COUPONS; ETC.) ARE ACCEPTABLE IN CROSSHATCHED AREA.
11. THE PWB FABRICATOR TO ADD TWO (2) BREAKAWAY V-GROOVED TOOLING STRIPS AS INDICATED BY THE CROSSHATCHED AREA ON THIS DRAWING. THE TOOLING STRIPS ARE TO HAVE FOUR (4) .157" +/-.002" DIAMETER NPTH IN THE CORNER LOCATIONS MARKED 'E'.



TITLE: CIRCUIT DRILL AND ETCH DRAWING	DOCUMENT NUMBER			
	SIZE: D	CODE: MD	NUMBER: 5024124-0-0	REV: AX00
	SCALE: 1:1	MEDIA: K	SHEET 2 OF 2	

WO#

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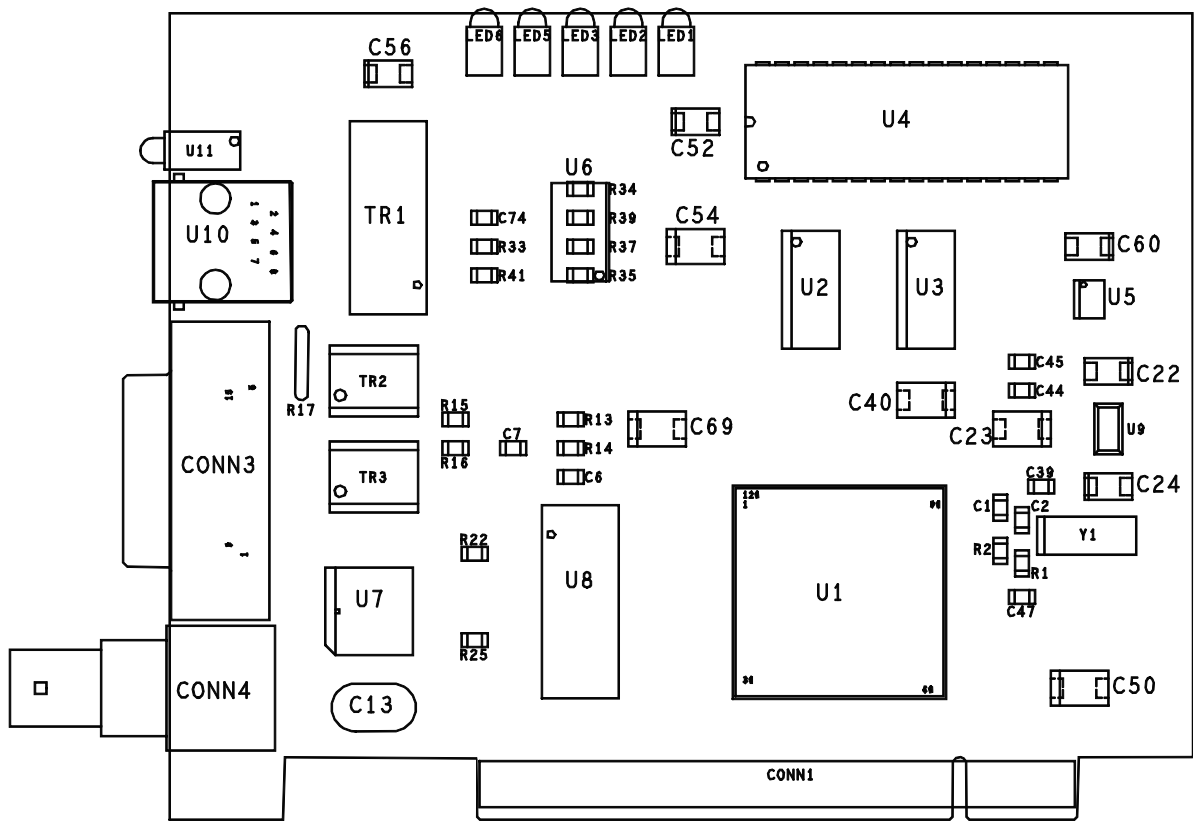

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TITLE: PTUB3_11

SIZE	CODE	NUMBER	REV
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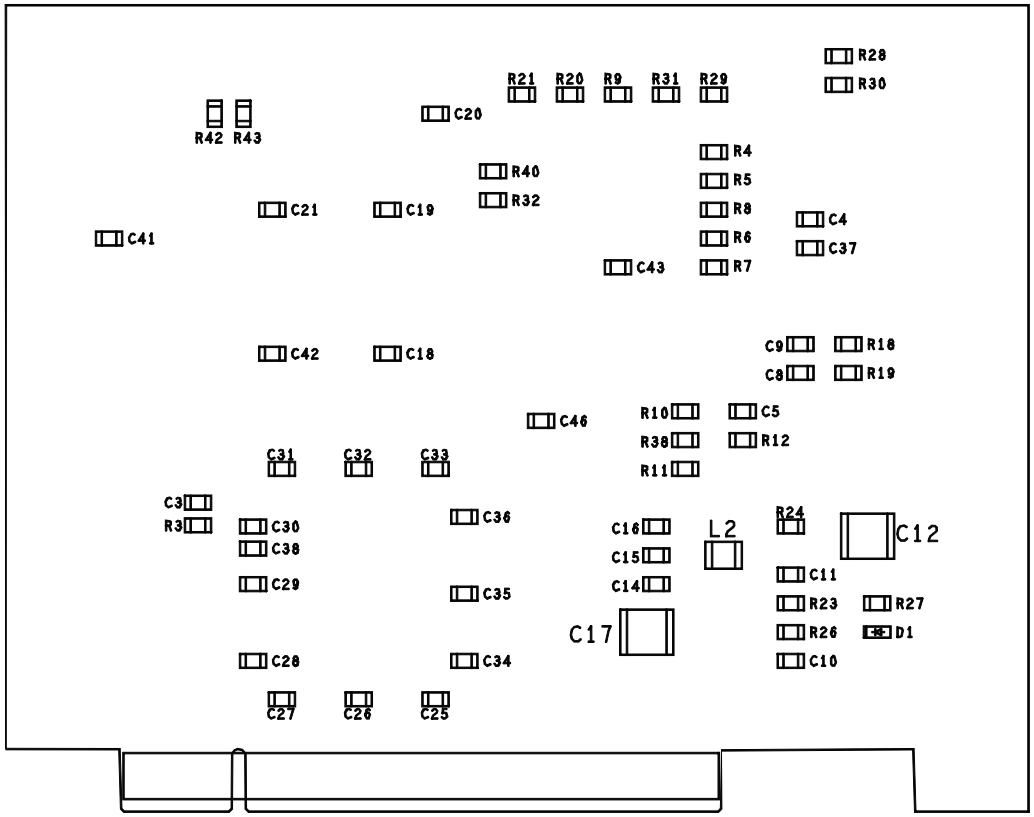

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TITLE: PTUB3_11

SIZE	CODE	NUMBER	REV
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